ANALOG-DIGITAL CONVERSION

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CHAPTER 8
DATA CONVERTER APPLICATIONS

SECTION 8.1: PRECISION MEASUREMENT AND SENSOR CONDITIONING

Introduction

The high resolution Σ-Δ measurement ADC has revolutionized the entire area of precision sensor signal conditioning and data acquisition. Modern Σ-Δ ADCs offer no-missing code resolutions to 24 bits, and greater than 19-bits of noise-free code resolution. The inclusion of on-chip PGAs coupled with the high resolution virtually eliminates the need for signal conditioning circuitry—the precision sensor can interface directly with the ADC in many cases.

As discussed in detail in Chapter 3 of this book, the Σ-Δ architecture is highly digitally intensive. It is therefore relatively easy to add programmable features and offer greater flexibility in their applications. Throughput rate, digital filter cutoff frequency, PGA gain, channel selection, chopping, and calibration modes are just a few of the possible features. One of the benefits of the on-chip digital filter is that its notches can be programmed to provide excellent 50-Hz/60-Hz power supply rejection. In addition, since the input to a Σ-Δ ADC is highly oversampled, the requirements on the antialiasing filter are not nearly as stringent as in the case of traditional Nyquist-type ADCs. Excellent common-mode rejection is also a result of the extensive utilization of differential analog and reference inputs. An important benefit of Σ-Δ ADCs is that they are typically designed on CMOS processes, therefore they are relatively low cost.

- **High Resolution**
  - **24 bits no missing codes**
  - **22 bits effective resolution (RMS)**
  - **19 bits noise-free code resolution (peak-to-peak)**
  - **On-Chip PGAs**
- **High Accuracy**
  - **INL 2ppm of Fullscale ~ 1LSB in 19 bits**
  - **Gain drift 0.5ppm/°C**
- **More Digital, Less Analog**
  - **Programmable Balance between Speed × Resolution**
- **Oversampling & Digital Filtering**
  - **50 / 60Hz rejection**
  - **High oversampling rate simplifies antialiasing filter**
- **Wide Dynamic Range**
- **Low Cost**

Figure 8.1: *Σ-Δ ADC Architecture Benefits*

In applying Σ-Δ ADCs, the user must accept the fact that because of the highly digital nature of the devices and the programmability offered, the digital interfaces tend to be more complex than with traditional ADC architectures such as successive approximation, for example. However, manufacturers' evaluation boards and associated development software along with complete data sheets can ease the overall design process considerably.

Some of the architectural benefits and features of the Σ-Δ measurement ADC are summarized in Figure 8.1 and 8.2.

- **Analog Input Buffer Options**
  - **Drives Σ–Δ Modulator, Reduces Dynamic Input Current**
- **Differential AIN, REFIN**
  - **Ratiometric Configuration Eliminates Need for Accurate Reference**
- **Multiplexer**
- **PGA**
- **Calibrations**
  - **Self Calibration, System Calibration, Auto Calibration**
- **Chopping Options**
  - **No Offset and Offset Drifts**
  - **Minimizes Effects of Parasitic Thermocouples**

Figure 8.2: *Σ-Δ System on Chip Features*

Applications of Precision Measurement Σ-Δ ADCs

High resolution measurement Σ-Δ ADCs find applications in many areas, including process control, sensor conditioning, instrumentation, etc. as shown in Figure 8.3. Because of the varied requirements, these ADCs are offered in a variety of configurations and options. For instance, Analog Devices currently (2004) has more than 24 different high resolution Σ-Δ ADC product offerings available. For this reason, it is impossible to cover all applications and products in a section of reasonable length, so we will focus on several representative sensor conditioning examples which will serve to illustrate most of the important application principles.

Because many sensors such as strain gages, flow meters, pressure sensors, and load cells use resistor-based circuits, we will use the AD7730 ADC as an example in a weigh scale design. A block diagram of the AD7730 is shown in Figure 8.4.

- Process Control
  - 4-20mA
- Sensors
  - Weigh Scale
  - Pressure
  - Temperature
- Instrumentation
  - Gas Monitoring
  - Portable Instrumentation
  - Medical Instrumentation

WEIGH SCALE

Figure 8.3: *Typical Applications of High Resolution Σ-Δ ADCs*

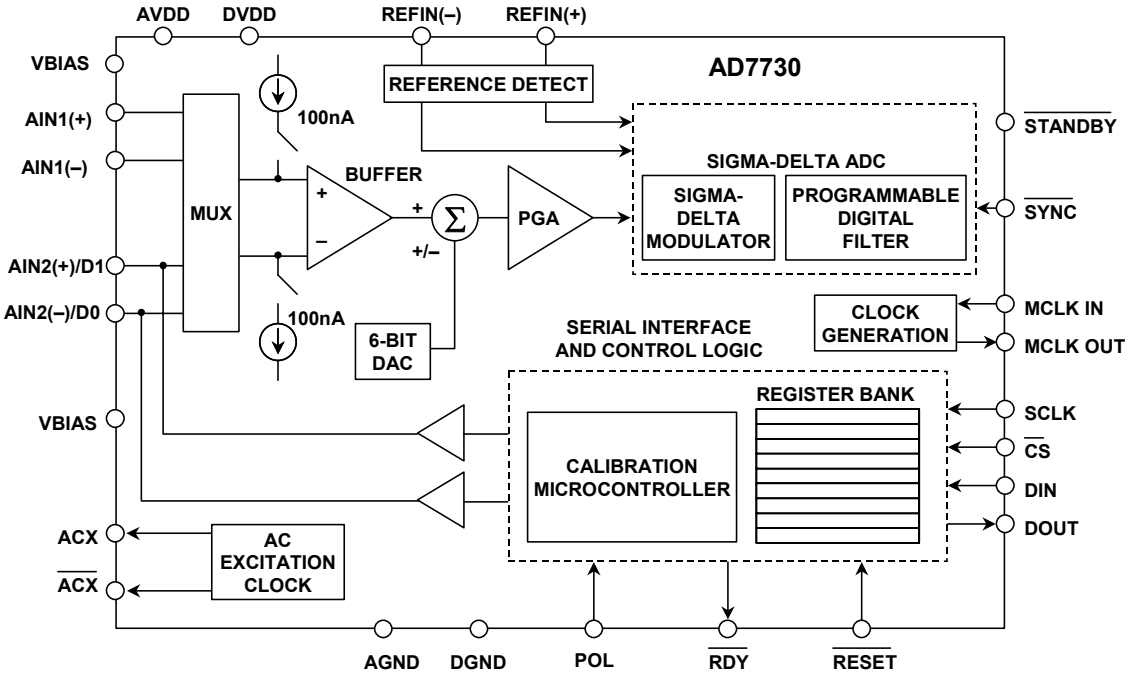


Figure 8.4: *AD7730 Single-Supply Bridge ADC*

The heart of the AD7730 is the 24-bit Σ-Δ core. The AD7730 is a complete analog front end for weigh-scale and pressure measurement applications. The device accepts low level signals directly from a transducer and outputs a serial digital word. The input signal is applied to a proprietary programmable gain front end based around an analog modulator. The modulator output is processed by a low pass programmable digital filter, allowing adjustment of filter cutoff, output rate and settling time. The response of the internal digital filter is shown in Figure 8.5.

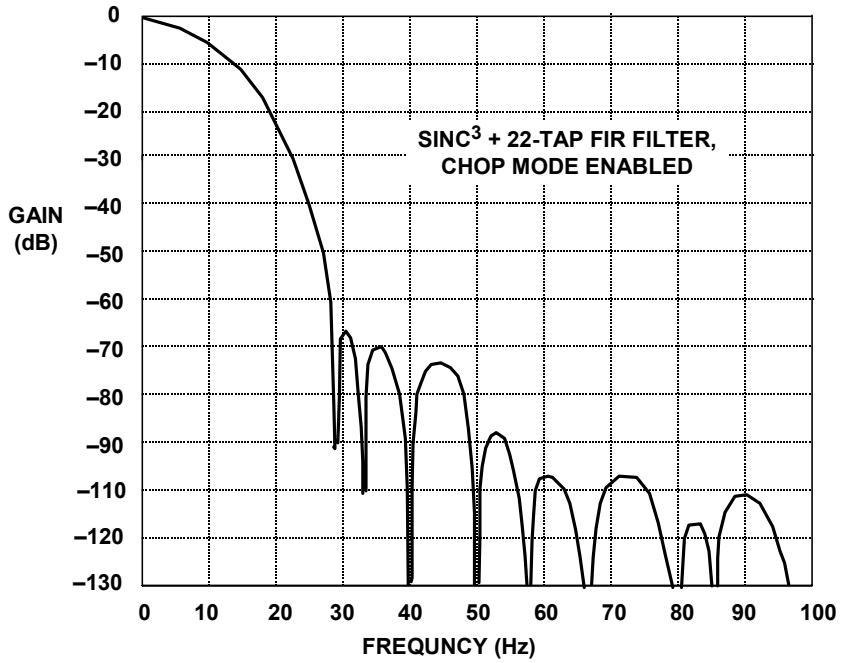


Figure 8.5: *AD7730 Digital Filter Frequency Response*

The part features two buffered differential programmable gain analog inputs as well as a differential reference input. The part operates from a single +5-V supply. It accepts four unipolar analog input ranges: 0 mV to +10 mV, +20 mV, +40 mV and +80 mV and four bipolar ranges: ±10 mV, ±20 mV, ±40 mV and ±80 mV. The peak-to-peak noise-free code resolution achievable directly from the part is 1 in 230,000 counts. An on-chip 6-bit DAC allows the removal of TARE voltages.

Clock signals for synchronizing ac excitation of the bridge are also provided. The serial interface on the part can be configured for three-wire operation and is compatible with microcontrollers and digital signal processors. The AD7730 contains self-calibration and system calibration options, and features an offset drift of less than 5 nV/°C and a gain drift of less than 2 ppm/°C.

The AD7730 is available in a 24-pin plastic DIP, a 24-lead SOIC and 24-lead TSSOP package. The AD7730L is available in a 24-lead SOIC and 24-lead TSSOP package. Key specifications for the AD7730 are summarized in Figure 8.6. Further details on the operation of the AD7730 can be found in References 1 and 2.

- **Resolution of 80,000 Counts Peak-to-Peak (16.5-Bits) for ± 10mV Fullscale Range**
- **Chop Mode for Low Offset and Drift**
- **Offset Drift: 5nV/°C (Chop Mode Enabled)**
- **Gain Drift: 2ppm/°C**
- **Line Frequency Common Mode Rejection: > 150dB**
- **Two-Channel Programmable Gain Front End**
- **On-Chip DAC for Offset/TARE Removal**
- **FASTStep Mode**
- **AC Excitation Output Drive**
- **Internal and System Calibration Options**
- **Single +5V Supply**
- **Power Dissipation: 65mW, (125mW for 10mV FS Range)**
- **24-Lead SOIC and 24-Lead TSSOP Packages**

Figure 8.6: *AD7730 Key Specifications*

A very powerful *ratiometric* technique which includes Kelvin sensing to minimize errors due to wiring resistance and also eliminates the need for an accurate excitation voltage is shown in Figure 8.7. The AD7730 measurement ADC can be driven from a single supply voltage which is also used to excite the remote bridge. Both the analog input and the reference input to the ADC are high impedance and fully differential. By using the + and – SENSE outputs from the bridge as the differential reference to the ADC, the reference voltage is proportional to the excitation voltage which is also proportional to the bridge output voltage. There is no loss in measurement accuracy if the actual bridge excitation voltage varies.

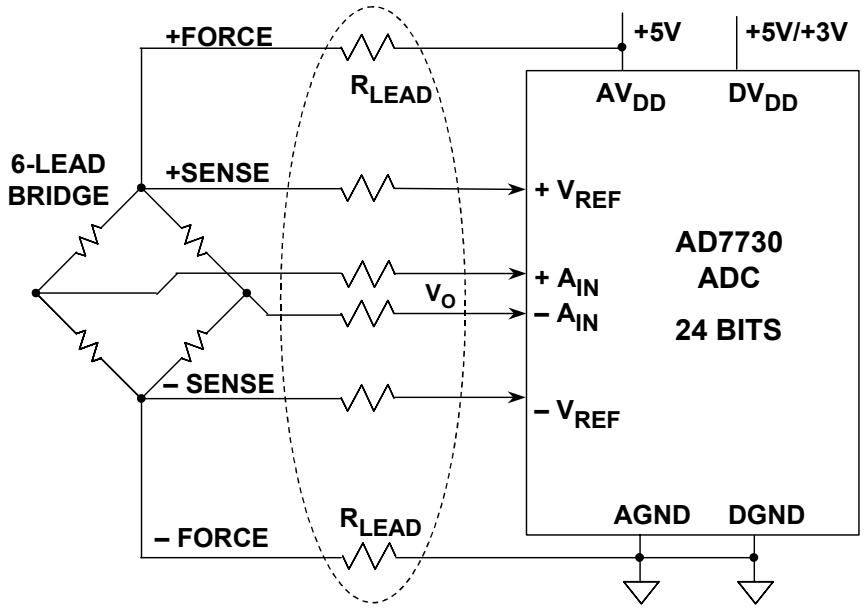


Figure 8.7: *AD7730 Bridge Application Showing Ratiometric Operation and Kelvin Sensing*

It should be noted that this ratiometric technique can be used in many applications where a sensor output is proportional to its excitation voltage or current, such as a thermistor or RTD.

Weigh Scale Design Analysis Using the AD7730 ADC

We will now proceed with a simple design analysis of a weigh scale based on the AD7730 ADC and a standard load cell. Figure 8.8 shows the overall design objectives for the weigh scale. The key specifications are the fullscale load (2 kg), and the resolution (0.1 g). These specifications primarily determine the basic load cell and ADC requirements.

- **Capacity** **2 kg**
- **Sensitivity** **0.1 g**

- **Other Features**
  - **Accuracy 0.1 %**
  - **Linearity ±0.1 g**
  - **Temp.Drift (±20ppm @ 10~30°C)**
  - **Speed (Readings / second)**
  - **Power (120V AC)**
  - **Dimensions (7.5"× 8.6" × 2.6")**
  - **Qualification ("Legal for Trade")**
- **Marketing**
  - **Price ($400)**

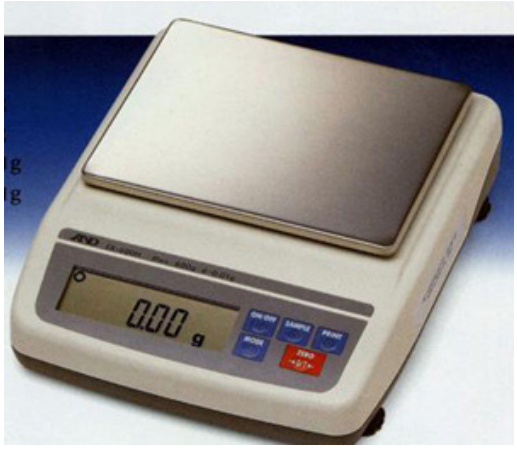


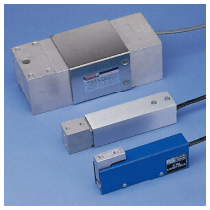
Figure 8.8: *Design Example—Weigh Scale*

The specifications of a load cell which matches the overall requirements are shown in Figure 8.9. Notice that the load cell is constructed with four individual strain gages connected in a standard bridge configuration. When the load is applied to the beam, R1 and R2 decrease in value, and R3 and R4 increase. This is popularly called the *four-element-varying* bridge configuration and is described in detail in Reference 1, Chapter 2.

The load cell selected has a fullscale load of 2 kg, and an output sensitivity of 2 mV/V. This means that with an excitation voltage of 10 V, the fullscale output voltage is 20 mV. Herein lies the major difficulty in load cell signal conditioning: accurately amplifying and digitizing the low level output signal without corrupting it with noise. The load cell output is analyzed further in Figure 8.10. With the chosen excitation voltage of 5 V, the fullscale bridge output voltage is only 10 mV. Notice that the output is also proportional to (or ratiometric with) the excitation voltage.

- **Full Load:** 2 kg
- **Sensitivity:** 2 mV/V
- **Excitation:** 10 V max

- **Other Features**
  - Impedance 350 Ω
  - Total Error 0.025 %
  - Hysteresis 0.025 %
  - Repeatability 0.01%
  - Temperature drift: 10ppm
  - Overload 150%
  - Dimensions
  - Cost ($200)



TYPICAL LOAD CELLS

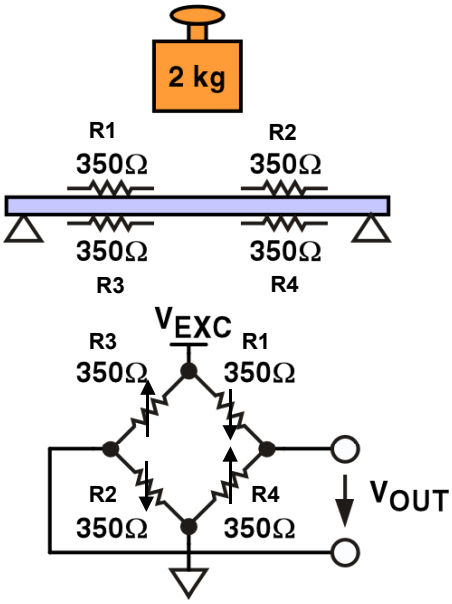


Figure 8.9: *Load Cell Characteristics*

- **Full Load:** 2 kg
- **Sensitivity:** 2 mV/V
- **Excitation:** 5 V

  - $V_{FS} = V_{EXC} \times$ Sensitivity
  - $V_{FS} = 5V \times 2mV/V = 10$ mV
  - $V_{CM} = 2.5$ V

- **Full-Scale Output Voltage: 10 mV**
- **Proportional to excitation voltage**
  - "Ratiometric"

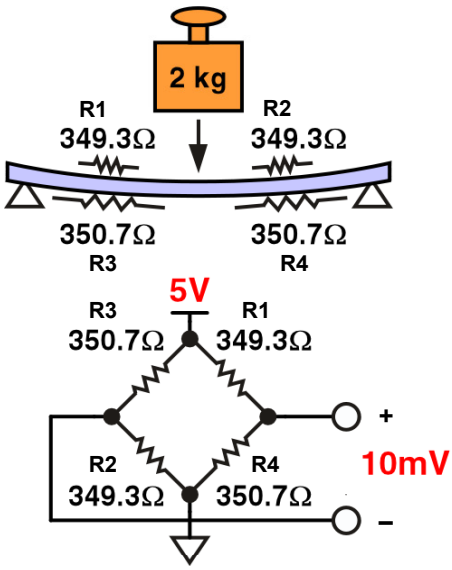


Figure 8.10: *Determining Fullscale Output of Load Cell with 5-V Excitation*

The next step is to determine the resolution requirements of the ADC, and the details are summarized in Figure 8.11. The total number of individual quantization levels (counts) required is equal to the fullscale weight (2 kg) divided by the desired resolution (0.1 g), or 20,000 counts. With a 5-V excitation voltage, the fullscale load cell output voltage is 10 mV for a 2-kg load.

The required noise-free resolution, V_{P-P}, is therefore given by V_{P-P} =10 mV/20,000 = 0.5 µV. This defines the code width, and therefore the peak-to-peak noise must be less than 0.5 µV. The corresponding allowable rms noise is given by $V_{RMS} = V_{P-P}/6.6$ = 0.5 µV/6.6 = 0.075-µV rms = 75-nV rms. (The factor 6.6 is used to convert peak-to-peak noise to rms noise, assuming Gaussian noise).

- **Required 0.1 g in 2 kg**
  - **# counts = full-scale / resolution**
  - **# counts = 2000 g / 0.1g = 20,000**
- **20,000 counts**
  - **V_{FS} = 10mV @ 5V excitation**
  - **$V_{P-P} = V_{FS}$ / # counts**
  - **V_{P-P} = 10mV / 20,000 = 0.0005mV**
- **0.5µV p-p noise**
  - **$V_{RMS} \approx V_{P-P}$ / 6.6**
  - **$V_{RMS} \approx$ 0.5µV / 6.6 = 0.075µV**
- **75nV RMS noise**
  - **Bits p-p = $\log_{10}(V_{FS} / V_{P-P}) / \log_{10}(2)$**
  - **Bits p-p = log(10mV / 0.0005mV) / 0.3**
- **14.3 bits p-p in 10mV range (Noise-free bits)**
  - **Bits RMS = $\log_{10}(V_{FS} / V_{RMS}) / \log_{10}(2)$**
  - **Bits RMS = $\log_{10}$(10mV / 0.000075) / 0.3**
- **17.0 bits RMS in 10mV range (Effective resolution)**

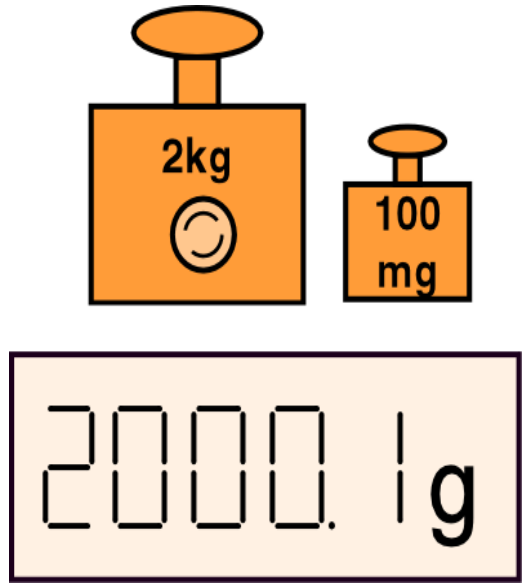


Figure 8.11: *Determining Resolution Requirements*

The noise-free code resolution of the ADC is calculated as follows:

$$\text{Noise-Free Code Resolution (Bits)} = \frac{\log_{10}\left(\frac{V_{FS}}{V_{PP}}\right)}{\log_{10}(2)}$$

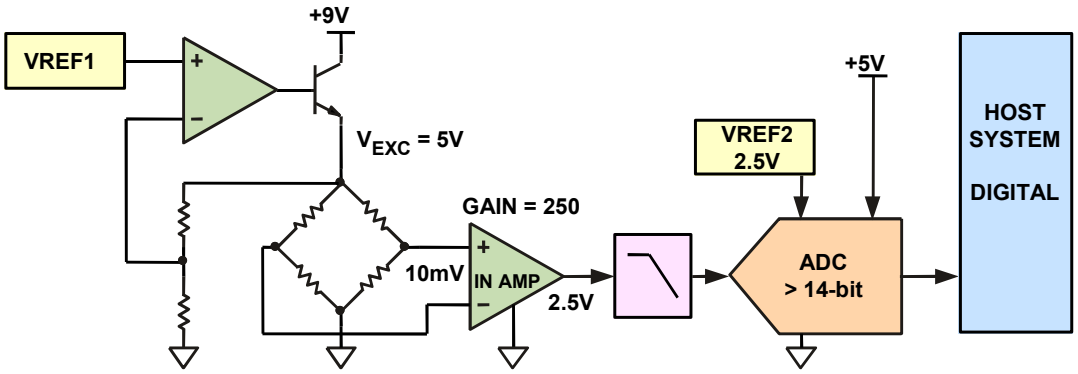
$$= \frac{\log_{10}\left(\frac{10\text{mV}}{0.5\mu\text{V}}\right)}{\log_{10}(2)} = 14.3 \text{ bits} \quad . \qquad \text{Eq. 8.1}$$

The effective resolution of the ADC is calculated as follows:

$$\text{Effective Resolution (Bits)} = \frac{\log_{10}\left(\frac{V_{FS}}{V_{PP}/6.6}\right)}{\log_{10}(2)}$$

$$= \frac{\log_{10}\left(\frac{10\text{mV}}{0.5\mu\text{V}/6.6}\right)}{0.3} = 17 \text{ bits.} \qquad \text{Eq. 8.2}$$

Figure 8.12 shows the traditional sensor conditioning solution to this problem, where an instrumentation amplifier is used to amplify the 10-mV fullscale bridge output signal to 2.5 V, which is compatible with the input of the14+ bit ADC. This approach requires a low-noise, low-drift in amp such as the AD620 precision in amp (Reference 4) which has a 0.1-Hz to 10-Hz peak-to-peak noise of 280 nV, approximately 280 nV ÷ 6.6 = 42-nV rms.



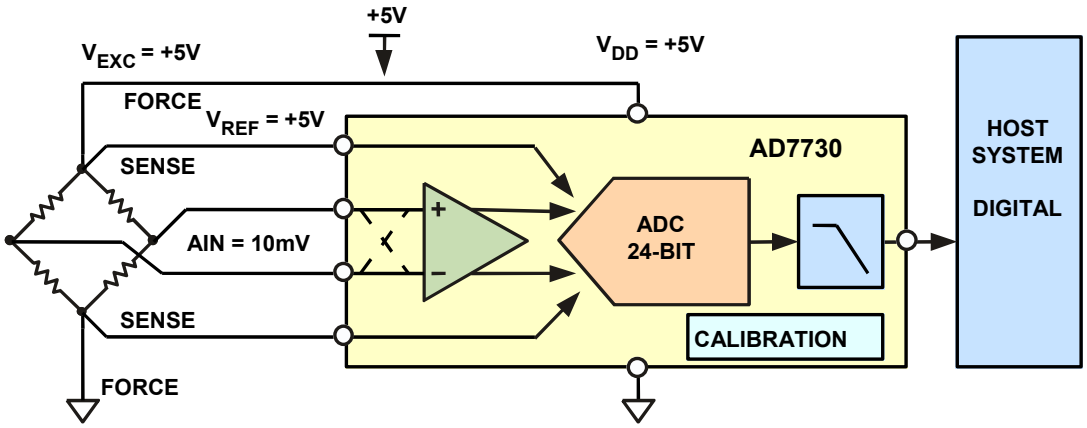
- **Complicated design**
- **Low pass filter is needed to keep low noise**
  - **For example, –3dB @ 10Hz, –60dB @ 50Hz (difficult filter design)**
- **Instrumentation amplifier performance is critical**
  - **Low noise (AD620: 0.28µV p-p noise in 0.1Hz to 10Hz BW is approximately 42nV RMS), low offset, low gain error**

Figure 8.12: *Traditional Approach to Design*

Another critical requirement of the system is a lowpass filter to remove noise and 50/60-Hz pickup. Assuming a signal 3-dB bandwidth of 10 Hz, the filter should be down at least 60 dB at 50 Hz—a challenging filter design to put it mildly! There are many other considerations in the design including the stability of the two reference voltages, the VREF1 buffer op amp, etc.

Finally, the ADC presents another serious challenge, requiring 14.3-bit noise-free code performance with a 2.5-V fullscale input signal—implying a 16-bit ADC with no more than approximately 3-LSBs peak-to-peak (0.45-LSBs rms) input-referred noise.

In order to avoid these traditional signal conditioning design problems, the AD7730-based design shown in Figure 8.13 represents a truly elegant solution requiring no instrumentation amplifier, reference, or filter. Note that the bridge interfaces directly with the AD7730 as previously shown in Figure 8.7. The AD7730 input PGA eliminates the need for an external in amp, providing a fullscale input range of 10 mV as a programmable option. Kelvin sensing is used to eliminate errors due to the wiring resistance in the bridge excitation lines. The bridge is driven directly from the +5-V supply, and the sense lines serve as the ADC reference voltage—thereby ensuring fully ratiometric operation as previously described. The need for a complicated filter is also eliminated—simple ceramic capacitor decoupling on each analog and reference input (not shown on the diagram) is sufficient.



- **AD7730 was designed for bridge transducers**
  - **Chopper, Buffer, PGA, Digital filter, tare DAC, Calibrations, …**
- **Fully Ratiometric, changes on $V_{EXC} = V_{REF}$ eliminated**
  - **Load ≈ V_{OUT} / V_{EXC}, AD7730 Data ≈ V_{IN} / V_{REF}, $V_{REF} = V_{EXC}$**

Figure 8.13: *Design Using AD7730*

System performance of the design can be determined by a detailed examination of the AD7730 data sheet, Table I and II, as shown in Figure 8.14. Table I shows the output rms noise in nV as a function of output data rate, digital filter 3-dB frequency, and input range (chopping mode enabled in all cases). An output data rate of 200-Hz yields a filter corner frequency of 7.9Hz which is reasonable for the application at hand. With an input range of ±10 mV, the output rms noise is 80 nV. This corresponds to a peak-to-peak noise, V_{PP} = 80 nV × 6.6 = 528 nV. The number of noise-free counts is obtained as V_{FS}/V_{PP} = 10 mV/ 528 nV =18,940. The system resolution for a 2-kg load is therefore 2 kg / 18,940 = 0.105 g, which is approximately the required specification of 0.1 g.

Table I. Output Noise vs. Input Range and Update Rate (CHP = 1)

				Typical Output RMS Noise in nV				
Output Data Rate	–3 dB Frequency	SF Word	Settling Time Normal Mode	Settling Time Fast Mode	Input Range = ±80 mV	Input Range = ±40 mV	Input Range = ±20 mV	Input Range = ±10 mV
50 Hz	1.97 Hz	2048	460 ms	60 ms	115	75	55	40
100 Hz	3.95 Hz	1024	230 ms	30 ms	155	105	75	60
150 Hz	5.92 Hz	683	153 ms	20 ms	200	135	95	70
200 Hz*	7.9 Hz	512	115 ms	15 ms	225	145	100	80
400 Hz	15.8 Hz	256	57.5 ms	7.5 ms	335	225	160	110

*Power-On Default

Table II. Peak-to-Peak Resolution vs. Input Range and Update Rate (CHP = 1)

				Peak-to-Peak Resolution in Counts (Bits)				
Output Data Rate	–3 dB Frequency	SF Word	Settling Time Normal Mode	Settling Time Fast Mode	Input Range = ±80 mV	Input Range = ±40 mV	Input Range = ±20 mV	Input Range = ±10 mV
50 Hz	1.97 Hz	2048	460 ms	60 ms	230k (18)	175k (17.5)	120k (17)	80k (16.5)
100 Hz	3.95 Hz	1024	230 ms	30 ms	170k (17.5)	125k (17)	90k (16.5)	55k (16)
150 Hz	5.92 Hz	683	153 ms	20 ms	130k (17)	100k (16.5)	70k (16)	45k (15.5)
200 Hz*	7.9 Hz	512	115 ms	15 ms	120k (17)	90k (16.5)	65k (16)	40k (15.5)
400 Hz	15.8 Hz	256	57.5 ms	7.5 ms	80k (16.5)	55k (16)	40k (15.5)	30k (15)

*Power-On Default

Figure 8.14: *AD7730 Resolution Determination From Data Sheet*

Table II can be also used to determine the noise-free code resolution which is 40,000 counts (15.5 noise-free bits) for a ±10-mV input range. This must be divided by a factor of 2 because only one-half the input range is used. Therefore, the actual design will provide approximately 20,000 counts (14.5 noise-free bits), which agrees closely with the previous calculation. The various calculations are summarized in Figure 8.15.

- **80nV RMS noise @ 200Hz**
  - $V_{P-P} \approx 6.6 \times V_{RMS}$
  - $V_{P-P} \approx 6.6 \times 80nV = 528nV$
  - $V_{FS} = 10mV$
  - # Counts = V_{FS} / V_{P-P}
  - # Counts = 10mV / 0.000528 = 18,940
  - Resolution = full scale / # counts
  - Resolution = 2,000g / 18,940 = 0.105g
- **0.105 g Resolution**

- **15.5 bits p-p in ±10mV (Noise-free bits)**
  - V_{FS} = 10mV ~ ½ of 20mV
  - Using only ½ of ADC input range
  - Losing 1 bit
- **14.5 bits p-p in 10mV**

- **40,000 counts in ±10mV**
  - V_{FS} = 10mV ~ ½ of 20mV
  - Using only ½ of ADC input range
- **20,000 counts in 10mV**

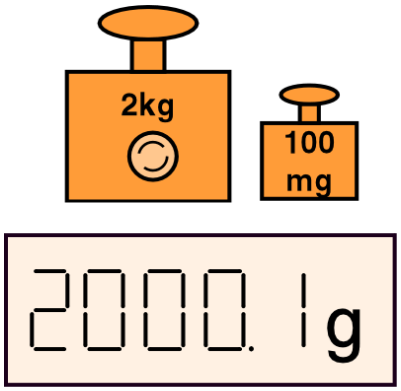


Figure 8.15: *AD7730 Resolution @ 200-Hz Data Rate*

Note that overall resolution can be increased by dropping back to lower output data rates with correspondingly lower digital filter corner frequencies.

Evaluation of the design is simplified with the AD7730 evaluation board and software as shown in Figure 8.16. The evaluation board can be connected directly to the load cell and the PC. The software allows the various AD7730 options to be varied to evaluate different combinations of data rates, filter frequencies, input ranges, chopping options, etc. Other ADCs in the AD77xx family have similar evaluation boards and software.

A summary of the final weigh scale design and specifications is shown in Figure 8.17.

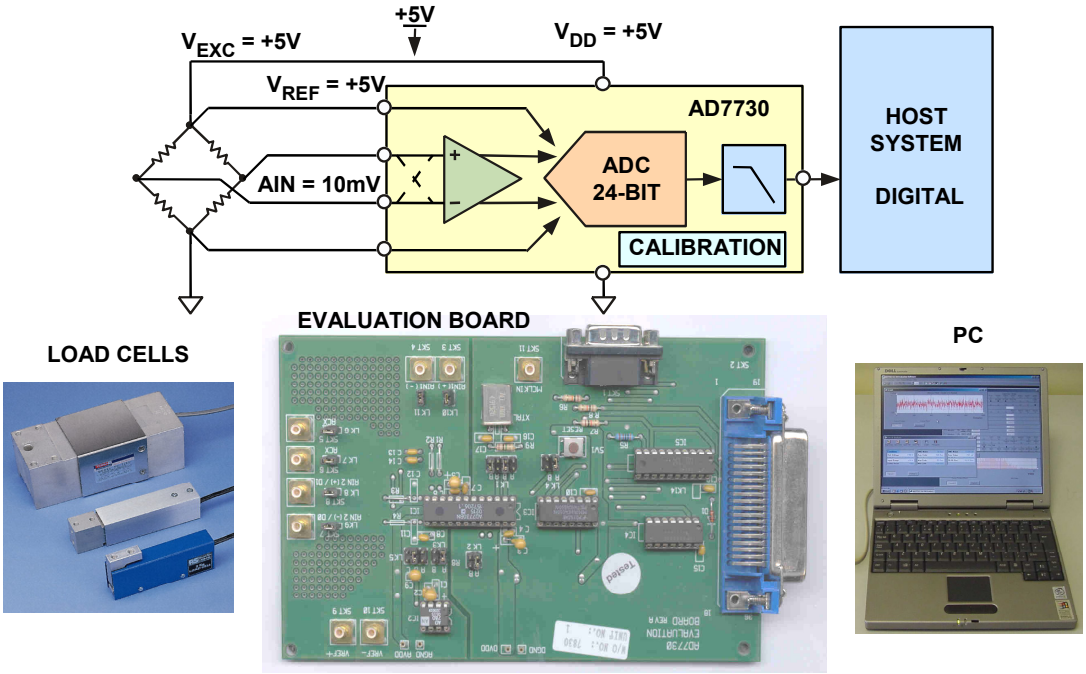


Figure 8.16: *Evaluation of Design Using Evaluation Board and Software*

	Required	Sensor Load Cell	Circuit AD7730	System Weigh Scale
Capacity	**2 kg**	**2 kg**	**AIN Range ±10mV**	**2 kg**
Sensitivity	**0.1g**	**2mV / V**	**Noise 80nV RMS**	**0.105g**

OUTPUT DATA RATE = 200Hz

Figure 8.17: *Final System Performance*

Thermocouple Conditioning Using the AD7793

Thermocouples provide accurate temperature measurements over an extremely wide range, however their relatively small output voltage makes the signal conditioning circuit design difficult. For instance, a Type K thermocouple has a nominal temperature coefficient of 39 µV/°C, so a temperature change of 1000°C produces only a 39-mV output voltage. The thermocouple does not measure temperature directly—its output voltage is proportional to the temperature difference between the actual measuring junction and the "cold" junction where the thermocouple wires are connected to the measuring electronics. (Details of thermocouple operation are described in Reference 1). Accurate thermocouple measurements therefore require that the temperature of the "cold" junction be measured in some manner to compensate for changes in ambient temperature.

The AD7793 dual channel 24-bit Σ-Δ is ideally suited for direct thermocouple measurements, and a simplified block diagram is shown in Figure 8.18 (Reference 5).

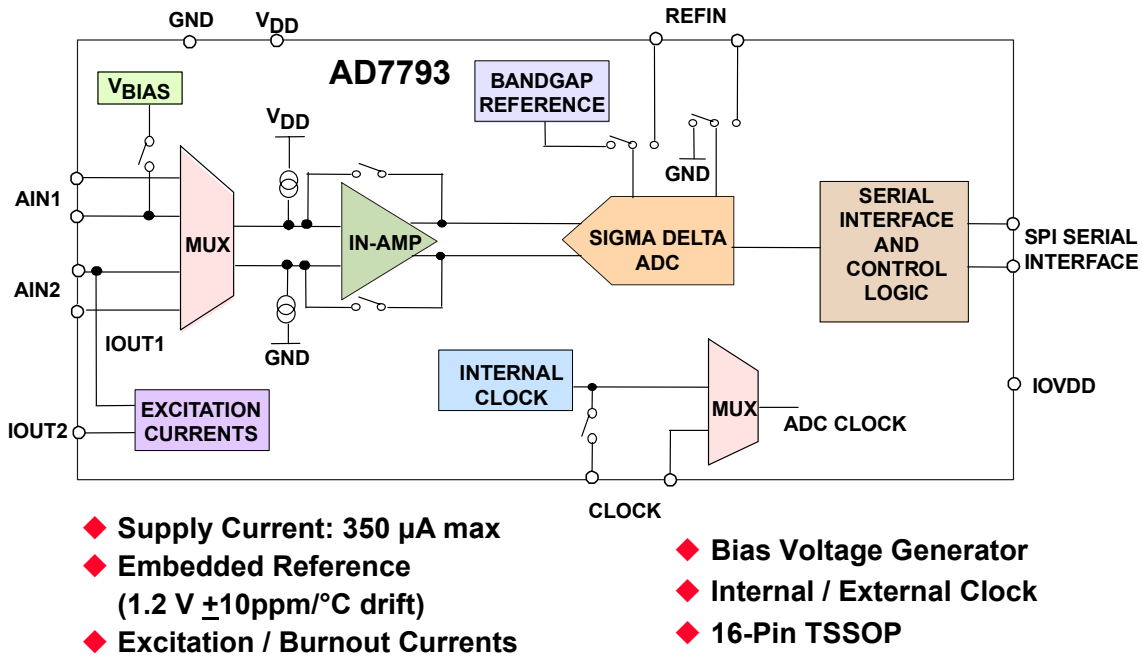
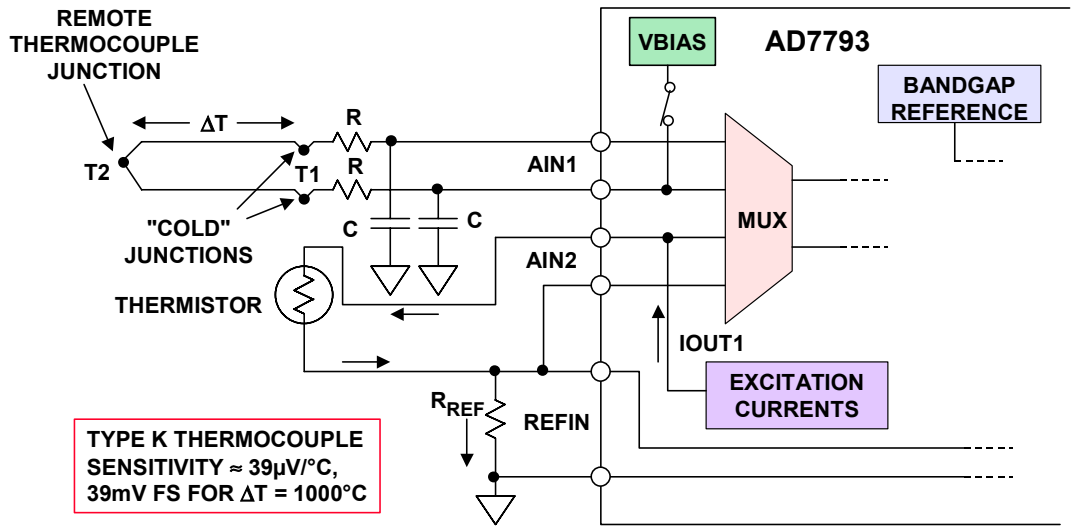


Figure 8.18: *AD7793 24-bit Σ-Δ ADC*

The AD7793 has two differential inputs, an on-chip in amp, reference voltage, bias voltage generator, and burnout/excitation current sources. Single-supply (+5 V) power supply current is 350-µA maximum.

A complete solution to a thermocouple measurement design is shown in Figure 8.19. Notice that a thermistor is used to measure the temperature of the "cold" junction via AIN2, and the thermocouple is connected directly to the AIN1 differential input. Note that the internal VBIAS voltage is used to establish the thermocouple common-mode voltage. The R/C filters minimize noise pickup from the remote thermocouple leads, and typical values of 100 Ω and 0.1 µF are reasonable choices.

The AD7793 is first programmed to measure the AIN1 thermocouple voltage using the internal 1.2-V bandgap voltage as a reference. This value is sent to a microcontroller connected to the serial interface. The voltage across the thermistor is established by the IOUT1 excitation current which also flows through a reference resistor, R_{REF}. The voltage developed across R_{REF} drives the auxillary reference input, REFIN. The AD7793 is programmed to use the REFIN reference when measuring the thermistor voltage at AIN2. The thermistor voltage is then sent to the microcontroller which performs the required calculations, including the correction for the temperature of the cold junction, T2. The thermistor is therefore connected in a ratiometric fashion such that variations in IOUT1 do not affect the accuracy of the thermistor measurement. Note that the powerful ratiometric technique will work with any resistive-based sensor including thermistors, bridges, strain gages, and RTDs.



- Bias voltage generator used to generate a common mode voltage for AIN1
- Current source provides current to thermistor for cold junction compensation and ratiometric operation using REFIN

Figure 8.19: *Thermocouple Design with Cold Junction Compensation using the AD7793*

Direct Digital Temperature Measurements

Temperature sensors which have digital outputs have a number of advantages over those with analog outputs, especially in remote applications. Opto-isolators can also be used to provide galvanic isolation between the remote sensor and the measurement system. A voltage-to-frequency converter driven by a voltage output temperature sensor accomplishes this function, however, more sophisticated ICs are now available which are more efficient and offer several performance advantages.

The TMP05/TMP06 digital output sensor family includes a voltage reference, V_{PTAT} generator, Σ-Δ ADC, and a clock source (see Figure 8.20). The sensor output is digitized by a first-order Σ-Δ modulator. This converter utilizes time-domain oversampling and a high accuracy comparator to deliver 12 bits of effective accuracy in an extremely compact circuit.

The output of the Σ-Δ modulator is encoded using a proprietary technique which results in a serial digital output signal with a mark-space ratio format (see Figure 8.21) that is easily decoded by any microprocessor into either degrees centigrade or degrees Fahrenheit, and readily transmitted over a single wire. Most importantly, this encoding method avoids major error sources common to other modulation techniques, as it is clock-independent.

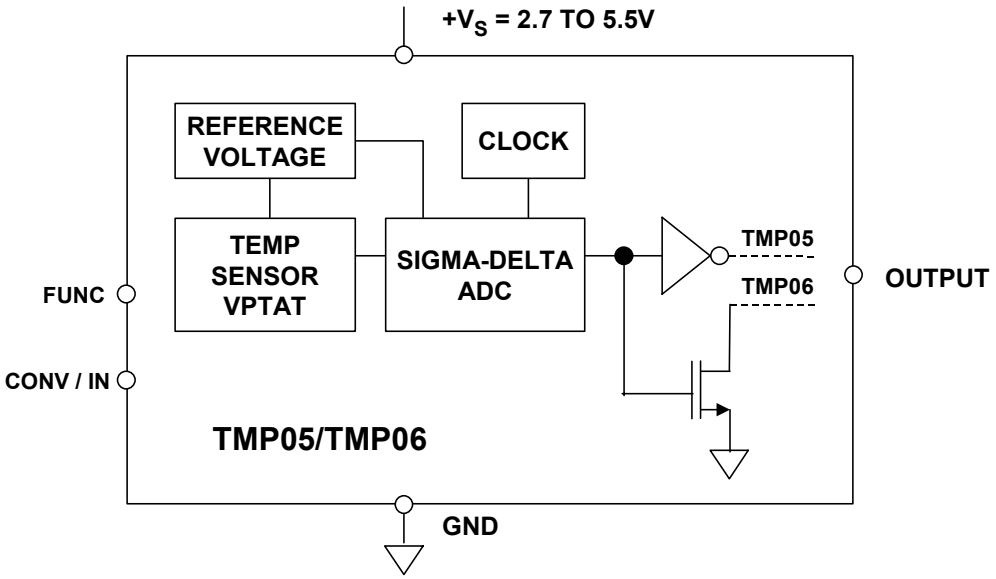
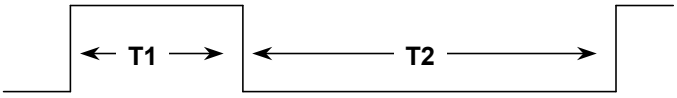


Figure 8.20: *Digital Output Temperature Sensors: TMP05/06*



$$\text{TEMPERATURE (°C)} = 406 - \left[\frac{731 \times T1}{T2}\right] \quad \text{FOR T1 + T2 = 30ms or 120ms}$$

$$\text{TEMPERATURE (°C)} = 406 - \left[\frac{91 \times T1}{T2}\right] \quad \text{FOR T1 + T2 = 100ms}$$

- **±0.5°C Accuracy from 0°C to +70°C**
- **0.025°C Resolution**
- **T1 + T2 = 120ms, 100ms, or 30ms (depending on status of CONV/IN pin**
- **Specified –40°C to +150°C**
- **+2.7V to +5.5V supply**
- **759µW Power Consumption @ 3.3V, Continuous Mode**
- **70µW Power Consumption @ 3.3V, One-Shot Mode(1Hz rate)**
- **5-pin SC-70 or SOT-23 Packages**

Figure 8.21: *TMP05/TMP06 Output Format*

The TMP05/TMP06 output is a stream of digital pulses, and the temperature information is contained in the mark-space ratio per the equations shown in Figure 8.21. The TMP05/TMP06 has 3 modes of operation. These are *continuously converting*, *daisy chain*, and *one shot*. A tri-state FUNC input selects one of the three possible modes. In the one shot mode, the power consumption is reduced to 70 µW at one sample per second.

The CONV/IN input is used to determine the rate with which the TMP05/TMP06 measures temperature in the *continuously converting* and *one shot* mode. In the daisy chain mode, the CONV/IN pin operates as the input to the daisy chain. The daisy chain mode allows multiple TMP05/TMP06s to be connected together and thus allow one input line of the microcontroller to be the sole receiver of all temperature measurements (see Reference 6 for further details).

Popular microcontrollers, such as the 80C51 and 68HC11, have on-chip timers which can easily decode the mark-space ratio of the TMP05/TMP06. A typical interface to the 80C51 is shown in Figure 8.22. Two timers, labeled *Timer 0* and *Timer 1* are 16 bits in length. The 80C51's system clock, divided by twelve, provides the source for the timers. The system clock is normally derived from a crystal oscillator, so timing measurements are quite accurate. Since the sensor's output is ratiometric, the actual clock frequency is not important. This feature is important because the microcontroller's clock frequency is often defined by some external timing constraint, such as the serial baud rate.

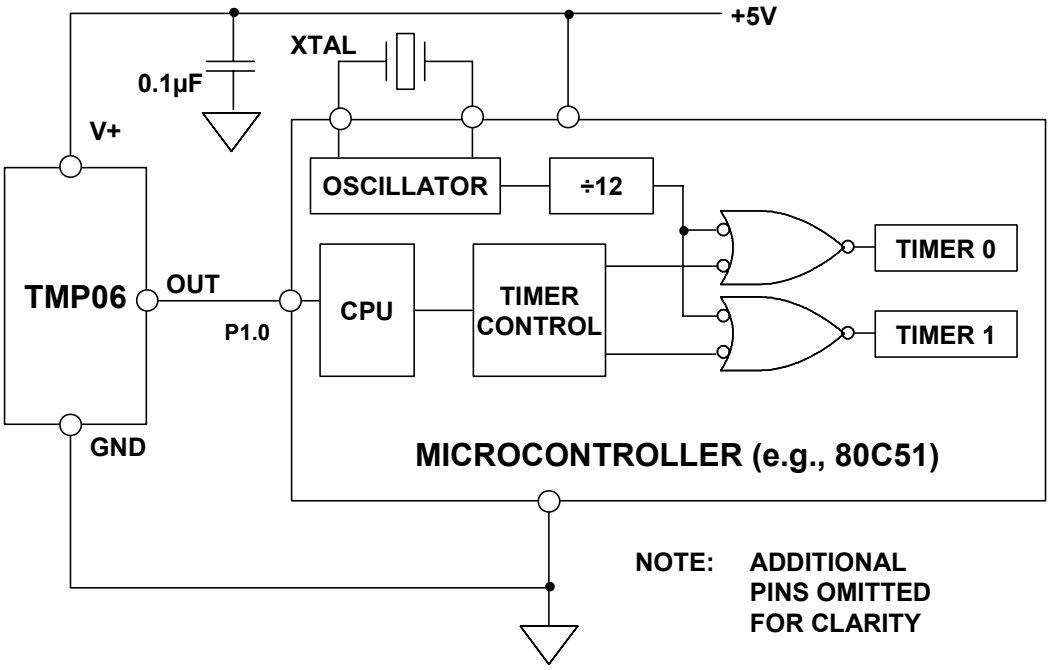


Figure 8.22: *Interfacing TMP06 to a Microcontroller*

Software for the sensor interface is straightforward. The microcontroller simply monitors I/O port P1.0, and starts *Timer 0* on the rising edge of the sensor output. The microcontroller continues to monitor P1.0, stopping *Timer 0* and starting *Timer 1* when the sensor output goes low. When the output returns high, the sensor's T1 and T2 times are contained in registers *Timer 0* and *Timer 1*, respectively. Further software routines can then apply the conversion factor shown in the equations above and calculate the temperature.

The TMP05/TMP06 are ideal for monitoring the thermal environment within electronic equipment. For example, the surface mounted package will accurately reflect the thermal conditions which affect nearby integrated circuits.

The TMP05 and TMP06 measure and convert the temperature at the surface of their own semiconductor chip. When they are used to measure the temperature of a nearby heat source, the thermal impedance between the heat source and the sensor must be considered. Often, a thermocouple or other temperature sensor is used to measure the temperature of the source, while the TMP05/TMP06 temperature is monitored by measuring the T1 and T2 pulse widths with a microcontroller. Once the thermal impedance is determined, the temperature of the heat source can be inferred from the TMP05/TMP06 output.

Carrying the integration a step further, we will now look at true temperature-to-digital converters. The basic bandgap reference (see complete discussion in Chapter 6 of this book) has been a building block for ADCs and DACs for many years, and most converters have them integrated on-chip. Inside the bandgap reference circuit, there is invariably a voltage or current which is proportional to absolute temperature (PTAT). There is no fundamental reason why this voltage or current cannot be used to sense the temperature of the IC substrate within the ADC. There is also no fundamental reason why the ADC cannot convert this voltage into a digital output word which represents the chip temperature. In the early days of IC data converters, internal power dissipation was considerable, so an internal temperature sensor would measure a temperature greater than the ambient temperature. Modern low voltage, low power ICs make it quite practical to use such a concept to produce a true temperature-to-digital converter which accurately reflects the ambient or PC board temperature.

This concept has expanded to an entire family of temperature-to-digital converters as well as ADCs with multiplexed inputs, where one input is the on-chip temperature sensor. This is a powerful feature, since modern microprocessor, DSP, and FPGA chips tend to dissipate lots of power, and most require a certain amount of airflow. A simple means of monitoring the PC board temperature is valuable in protecting these critical circuits against damage from excessive temperatures due to fault conditions.

The ADT7301 is a 13-bit digital temperature sensor with a 14th bit as a sign bit (Reference 7). The part contains an on-chip bandgap reference, temperature sensor, a 13-bit ADC, and serial interface logic functions in SOT-23 and MSOP packages. The ADC section consists of a conventional successive-approximation converter based on a switched capacitor DAC architecture. The parts are capable of running on a +2.7-V to +5.5-V power supply. The on-chip temperature sensor allows an accurate measurement of the ambient device temperature to be made. The specified measurement range of the ADT7301 is –40°C to +150°C. It is not recommended to operate the device at temperatures above +125°C for greater than a total of 5% of the projected lifetime of the device. Any exposure beyond this limit will affect device reliability. A simplified block diagram of the ADT7301 is given in Figure 8.23, and key specifications are summarized in Figure 8.24.

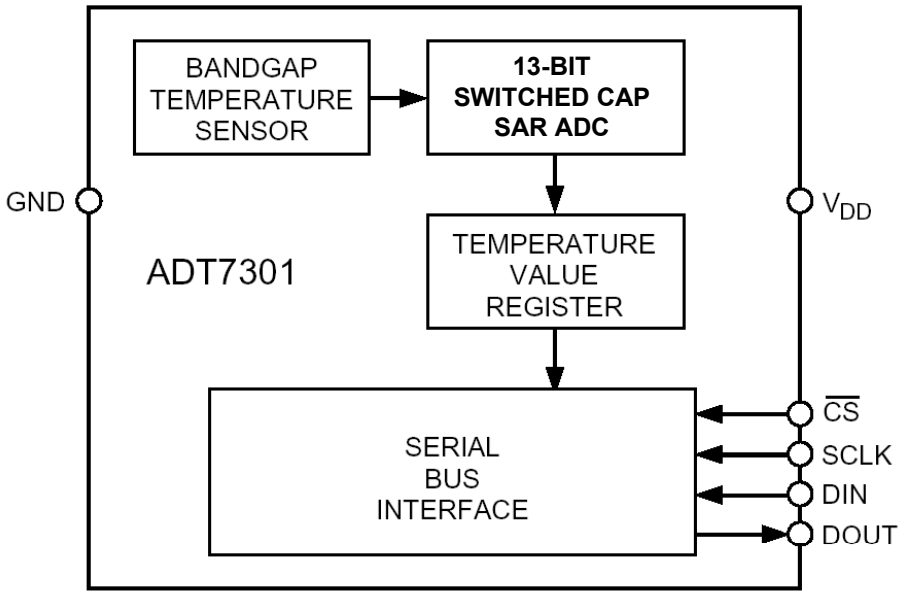


Figure 8.23: *ADT7301 13-Bit, ±0.5°C Accurate, Micropower Digital Temperature Sensor*

- **13-Bit Temperature-to-Digital Conversion**
- **–40°C to +150°C Operating Temperature Range**
- **±0.5°C Accuracy**
- **0.03125°C Temperature Resolution**
- **+2.7V to +5.5V Supply**
- **4.88µW Power Dissipation, for 1 sample/second Conversion Rate**
- **Serial Interface**
- **6-Lead SOT-23 or 8-Lead SOIC Package**

Figure 8.24: *ADT7301 Key Specifications*

The ADT7301 can be used for surface or air-temperature sensing applications. If the device is cemented to a surface with thermally conductive adhesive, the die temperature will be within about 0.1°C of the surface temperature, thanks to the device's low power consumption. Care should be taken to insulate the back and leads of the device from airflow, if the ambient air temperature is different from the surface temperature being measured. The ground pin provides the best thermal path to the die, so the temperature of the die will be close to that of the printed circuit ground track. Care should be taken to ensure that this is in good thermal contact with the surface being measured.

As with any IC, the ADT7301 and its associated wiring and circuits must be kept free from moisture to prevent leakage and corrosion, particularly in cold conditions where condensation is more likely to occur. Water-resistant varnishes and conformal coatings can be used for protection. The small size of the ADT7301 package allows it to be mounted inside sealed metal probes, which provide a safe environment for the device.

Microprocessor Substrate Temperature Sensors

Today's computers require that hardware as well as software operate properly, in spite of the many things that can cause a system crash or lockup. The purpose of hardware monitoring is to monitor the critical items in a computing system and take corrective action should problems occur.

Microprocessor supply voltage and temperature are two critical parameters. If the supply voltage drops below a specified minimum level, further operations should be halted until the voltage returns to acceptable levels. In some cases, it is desirable to reset the microprocessor under "brownout" conditions. It is also common practice to reset the microprocessor on power-up or power-down. Switching to a battery backup may be required if the supply voltage is low.

Under low voltage conditions it is mandatory to inhibit the microprocessor from writing to external CMOS memory by inhibiting the Chip Enable signal to the external memory.

Many microprocessors can be programmed to periodically output a "watchdog" signal. Monitoring this signal gives an indication that the processor and its software are functioning properly and that the processor is not stuck in an endless loop.

The need for hardware monitoring has resulted in a number of ICs, traditionally called "microprocessor supervisory products," which perform some or all of the above functions. These devices range from simple manual reset generators (with debouncing) to complete microcontroller-based monitoring sub-systems with on-chip temperature sensors and ADCs. Analog Devices' ADM-family of products is specifically to perform the various microprocessor supervisory functions required in different systems.

CPU temperature is critically important in the Pentium microprocessors. For this reason, all new Pentium devices have an on-chip substrate PNP transistor which is designed to monitor the actual chip temperature. The collector of the substrate PNP is connected to the substrate, and the base and emitter are brought out on two separate pins of the Pentium.

The ADM1023 Microprocessor Temperature Monitor is specifically designed to process these outputs and convert the voltage into a digital word representing the chip temperature. It is optimized for use with the Pentium®III microprocessor. The simplified analog signal processing portion of the ADM1023 is shown in Figure 8.25.

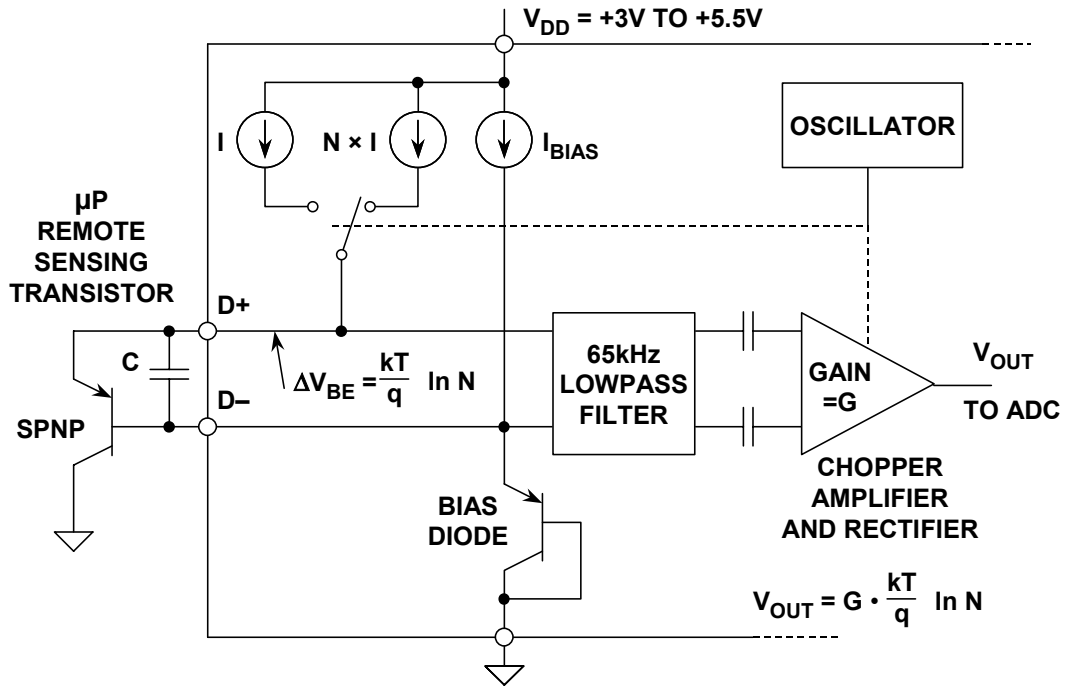


***Figure 8.25**: ADM1023 Microprocessor Temperature Monitor Input Conditioning Circuits*

The technique used to measure the temperature is identical to the "ΔV_{BE}" principle previously discussed in Chapter 7 of this book. Two different currents (I and N·I) are applied to the sensing transistor, and the voltage measured for each. The change in the base-emitter voltage, ΔV_{BE}, is a PTAT voltage and given by the equation:

$$\Delta V_{BE} = \frac{kT}{q} \ln(N) . \qquad \text{Eq. 8.3}$$

Figure 8.25 shows the external sensor as a substrate PNP transistor, provided for temperature monitoring in the microprocessor, but it could equally well be a discrete transistor such as a 2N3904 or 2N3906. If a discrete transistor is used, the collector should be connected to the base and not grounded. To prevent ground noise interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode. If the sensor is operating in a noisy environment, C may be optionally added as a noise filter. Its value is typically 2200 pF, but should be no more than 3000 pF.

To measure ΔV_{BE}, the sensing transistor is switched between operating currents of I and N·I. The resulting waveform is passed through a 65-kHz lowpass filter to remove noise, then to a chopper-stabilized amplifier which performs the function of amplification and synchronous rectification. The resulting dc voltage is proportional to ΔV_{BE} and is digitized by the ADC and stored as an 11-bit word. To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles.

In addition, the ADM1023 contains an on-chip temperature sensor, and its signal conditioning and measurement is performed in the same manner.

One LSB of the ADM1023 corresponds to 0.125ºC, and the ADC can theoretically measure from 0°C to +127.875ºC. The results of the local and remote temperature measurements are stored in the local and remote temperature value registers, and are compared with limits programmed into the local and remote high and low limit registers as shown in Figure 8.26. An $\overline{\text{ALERT}}$ output signals when the on-chip or remote temperature is out of range. This output can be used as an interrupt, or as an SMBus alert.

The limit registers can be programmed, and the device controlled and configured, via the serial System Management Bus (SMBus). The contents of any register can also be read back by the SMBus. Control and configuration functions consist of: switching the device between normal operation and standby mode, masking or enabling the $\overline{\text{ALERT}}$ output, and selecting the conversion rate which can be set from 0.0625 Hz to 8 Hz. Key specifications for the ADM1023 are given in Figure 8.27.

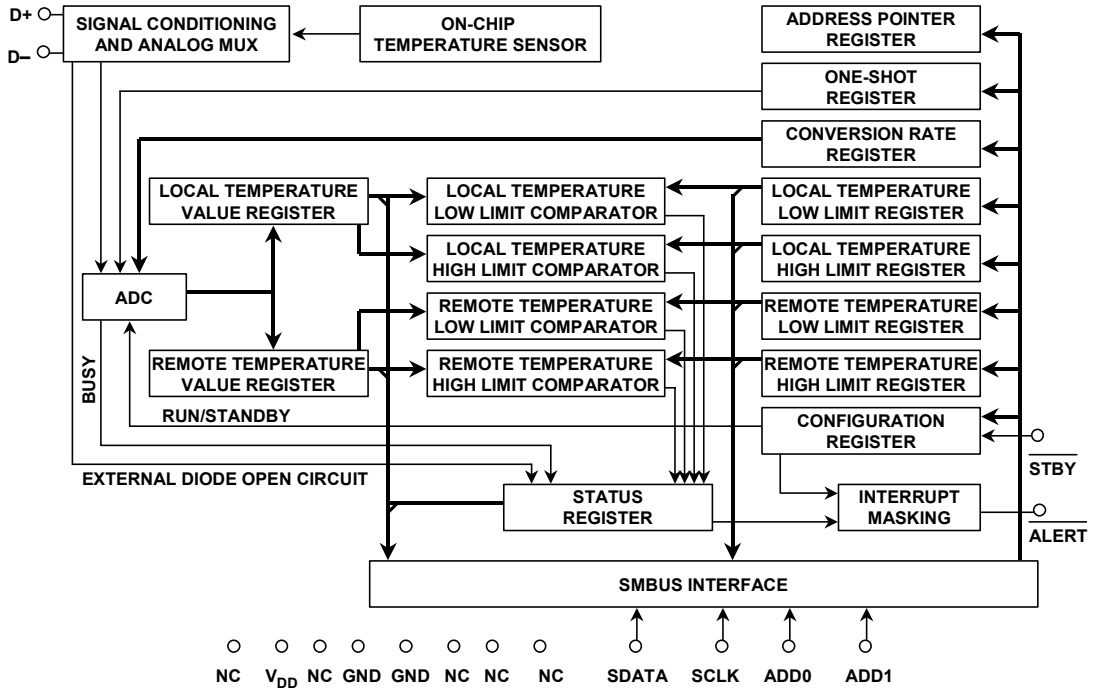


Figure 8.26: *ADM1023 Simplified Block Diagram*

- **On-Chip and Remote Microprocessor Sensing**
- **Offset Registers for System Calibration**
- **1°C Accuracy and Resolution on Local Channel**
- **0.125°C Resolution/1°C Accuracy on Remote Channel**
- **Programmable Over/Under Temperature Limits**
- **Programmable Conversion Rate**
- **Supports System Management Bus (SMBus) Alert**
- **2-Wire SMBus Serial Interface**
- **200µA Max. Operating Current (0.25 Conversions/Second)**
- **1µA Standby Current**
- **+3V to +5.5V Supply**
- **16-Lead QSOP Package**

Figure 8.27: *ADM1023 Key Specifications*

Applications of ADCs in Power Meters

While electromechanical energy meters have been popular for over 50 years, a solid-state energy meter delivers far more accuracy and flexibility. Just as important, a well designed solid-state meter will have a longer useful life. The ADE775x energy metering ICs are a family products designed to implement this type of meter (References 9, 10, 11).

We must first consider the fundamentals of power measurement (see Figure 8.28). Instantaneous AC voltage is given by the expression $v(t) = V\times\cos(\omega t)$, and the current (assuming it is in phase with the voltage) by $i(t) = I\times\cos(\omega t)$. The *instantaneous power* is the product of v(t) and i(t):

$$p(t) = V\times I\times\cos^2(\omega t) \qquad \text{Eq. 8.4}$$

Using the trigonometric identity, $2\cos^2(\omega t) = 1 + \cos(2\omega t)$, Eq. 8.5

$$p(t) = \frac{V\times I}{2}\left[1+\cos(2\omega t)\right] = \text{Instantaneous Power.} \qquad \text{Eq. 8.6}$$

The *instantaneous real power* is simply the average value of p(t). It can be shown that computing the instantaneous real power in this manner gives accurate results even if the current is not in phase with the voltage (i.e., the power factor is not unity. By definition, the power factor is equal to $\cos\theta$, where θ is the phase angle between the voltage and the current). It also gives the correct real power if the waveforms are non-sinusoidal.

- $v(t) = V \times \cos(\omega t)$ (Instantaneous Voltage)
- $i(t) = I \times \cos(\omega t)$ (Instantaneous Current)
- $p(t) = V \times I \cos^2(\omega t)$ (Instantaneous Power)
- $p(t) = \frac{V \times I}{2}\left[1 + \cos(2\omega t)\right]$

Average Value of p(t) = Instantaneous *Real Power*

Includes Effects of Power Factor and Waveform Distortion

Figure 8.28: *Basics of Power Measurements*

The ADE7755 implements these calculations, and a block diagram is shown in Figure 8.29. The two ADCs digitize the voltage signals from the current and voltage transducers. These ADCs are 16-bit second order Σ-Δ with an input sampling rate of 900 kSPS. This analog input structure greatly simplifies transducer interfacing by providing a wide dynamic range for direct connection to the transducer and also by simplifying the antialiasing filter design. A programmable gain stage in the current channel further facilitates easy transducer interfacing. A high-pass filter in the current channel removes any dc component from the current signal. This eliminates any inaccuracies in the real power calculation due to offsets in the voltage or current signals.

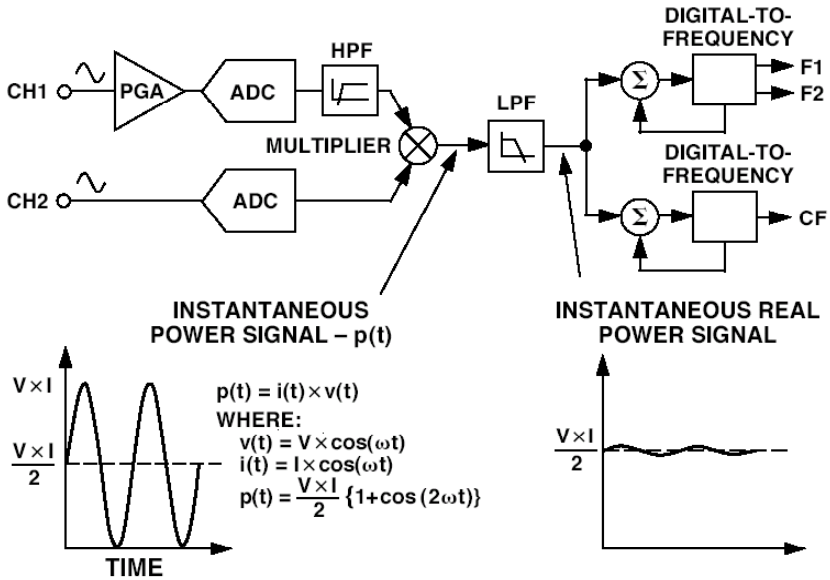


Figure 8.29: *ADE7755 Energy Metering IC Signal Processing*

The real power calculation is derived from the instantaneous power signal. The instantaneous power signal is generated by a direct multiplication of the current and voltage signals. In order to extract the real power component (i.e., the dc component), the instantaneous power signal is low-pass filtered. Figure 8.29 illustrates the instantaneous real power signal and shows how the real power information can be extracted by low-pass filtering the instantaneous power signal. This method correctly calculates real power for non-sinusoidal current and voltage waveforms at all power factors. All signal processing is carried out in the digital domain for superior stability over temperature and time.

The low-frequency output of the ADE7755 is generated by accumulating this real power information (see Figure 8.30). This low frequency inherently means a long accumulation time between output pulses. The output frequency is therefore proportional to the average real power. This average real power information can, in turn, be accumulated (e.g., by a counter) to generate real energy information. Because of its high output frequency and shorter integration time, the CF output is proportional to the instantaneous real power. This is useful for system calibration purposes that would take place under steady load conditions.

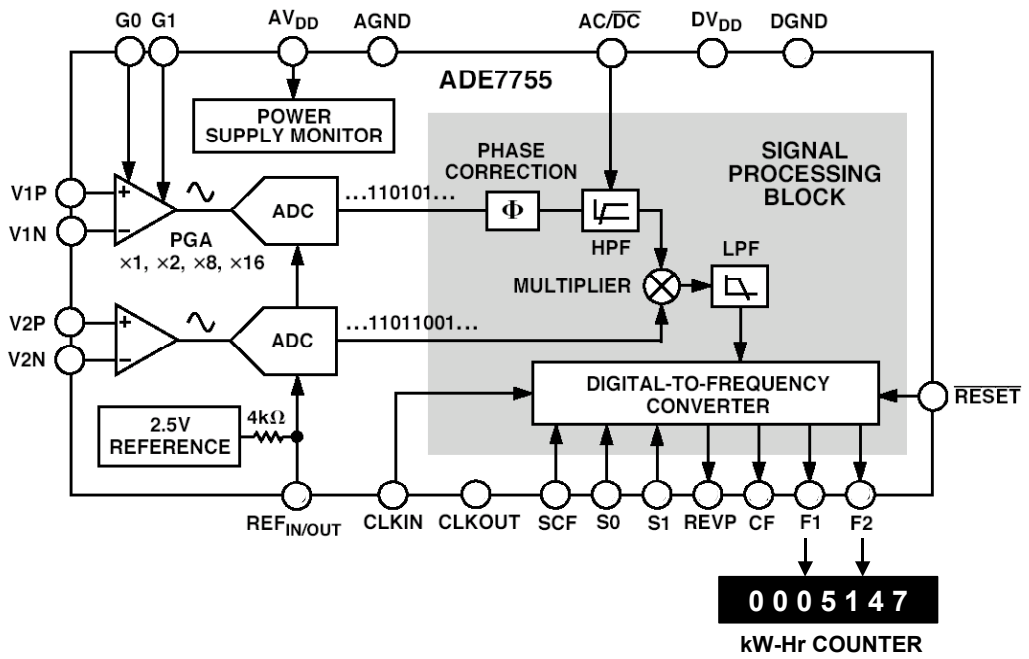


Figure 8.30: *ADE7755 Energy Metering IC with Pulse Output*

Figure 8.31 shows a typical connection diagram for Channel V1 and V2. A CT (current transformer) is the transducer selected for sensing the Channel V1 current. Notice the common-mode voltage for Channel 1 is AGND and is derived by center tapping the burden resistor to AGND. This provides the complementary analog input signals for V1P and V1N. The CT turns ratio and burden resistor Rb are selected to give a peak differential voltage of ±470 mV/Gain at maximum load. The Channel 2 voltage sensing is accomplished with a PT (potential transformer) to provide complete isolation from the power line.

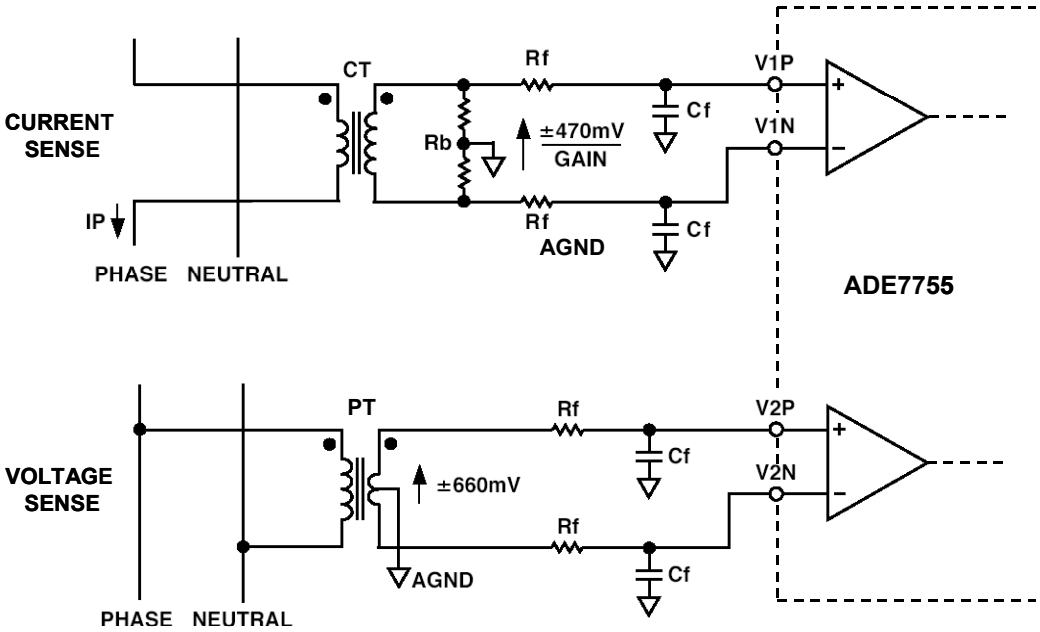


Figure 8.31: *Typical Connections for Channel 1 (Current Sense) and Channel 2 (Voltage Sense)*

REFERENCES:
8.1 PRECISION MEASUREMENT AND SENSOR CONDITIONING

1. Walt Kester, **Practical Design Techniques for Sensor Signal Conditioning**, Analog Devices, 1999, Chapter 8. Available for download at http://www.analog.com.

2. Data sheet for AD7730/AD7730L Bridge Transducer ADC, http://www.analog.com.

3. Walter G. Jung, **Op Amp Applications**, Analog Devices, 2002, ISBN 0-916550-26-5, Chapter 4.

4. Data sheet for AD620 Precision Instrumentation Amplifier, http://www.analog.com.

5. Data sheet for AD7793 24-bit Dual Sigma-Delta ADC, http://www.analog.com.

6. Data sheet for TMP05/TMP06 ±0.5°C Accurate PWM Temperature Sensor in 5-Lead SC-70, http://www.analog.com.

7. Data sheet for ADT7301 13-bit, ±0.5°C Accurate, MicroPower Digital Temperature Sensor, http://www.analog.com.

8. Data sheet for ADM1023 ACPI Compliant High Accuracy Microprocessor System Temperature Monitor, http://www.analog.com.

9. Data sheet for ADE7755 Energy Metering IC with Pulse Output, http://www.analog.com.

10. Paul Daigle, "All-Electronic Power and Energy Meters," **Analog Dialogue**, Volume 33, Number 2, February, 1999, http://www.analog.com.

11. John Markow, "Microcontroller-Based Energy Metering using the AD7755," **Analog Dialogue**, Volume 33, Number 9, October, 1999, http://www.analog.com.

SECTION 8.2: MULTICHANNEL DATA ACQUISITION SYSTEMS

Walt Kester

Data Acquisition System Configurations

There are many applications for data acquisition systems in measurement and process control. All data acquisition applications involve digitizing analog signals for analysis using ADCs. In a measurement application, the ADC is followed by a digital processor which performs the required data analysis. In a process control application, the process controller generates feedback signals which typically must be converted back into analog form using a DAC.

Although a single ADC digitizing a single channel of analog data constitutes a data acquisition system, the term *data acquisition* generally refers to multichannel systems. If there is feedback from the digital processor, DACs may be required to convert the digital responses into analog. This process is often referred to as *data distribution*.

Figure 8.32A shows a data acquisition/distribution process control system where each channel has its own dedicated ADC and DAC. An alternative configuration is shown in Figure 8.32B, where analog multiplexers and demultiplexers are used with a single ADC and DAC. In most cases, especially where there are many channels, this second configuration provides an economical alternative.

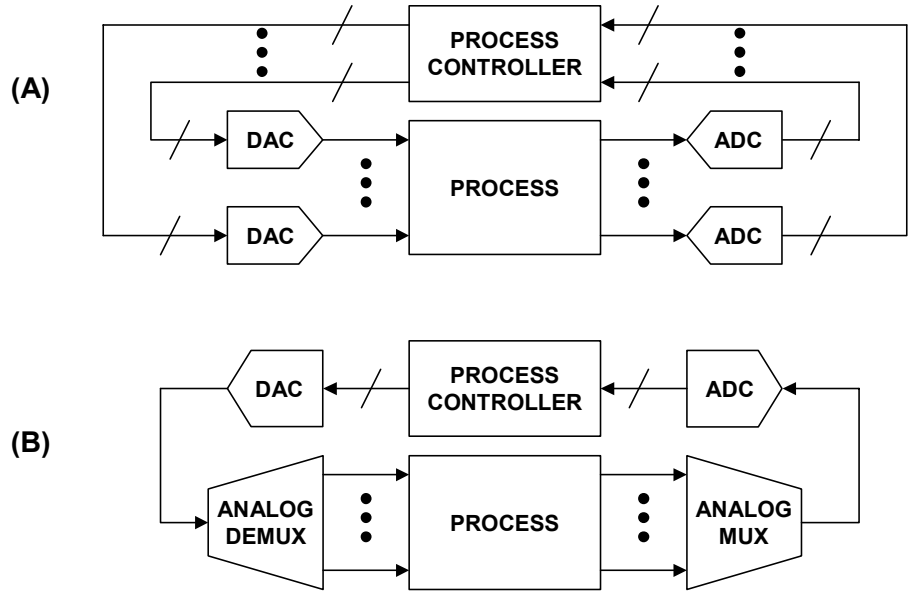


Figure 8.32: *Two Approaches to a Multichannel Data Acquisition System*

There are many tradeoffs involved in designing a data acquisition system. Issues such as filtering, amplification, multiplexing, demultiplexing, sampling frequency, and partitioning must be resolved.

Multiplexing

Multiplexing is a fundamental part of a data acquisition system as shown in Figure 8.32. Multiplexers and switches are examined in more detail in Reference 1, but a fundamental understanding is required to design a data acquisition system—even if the multiplexer is on the same chip as the ADC, which is often the case today.

A simplified diagram of an analog multiplexer is shown in Figure 8.33. The number of input channels typically ranges from 2 to 32, and the devices are generally fabricated on CMOS processes. Most multiplexers have internal channel-address decoding logic and registers, but in a few, these functions must be performed externally. Unused multiplexer inputs *must* be grounded or severe loss of system accuracy may result. The key specifications are *switching time*, *on-resistance*, *on-resistance modulation*, and *off-channel isolation (crosstalk)*. For a detailed discussion of the details of analog multiplexers, refer to Chapter 7 of this book.

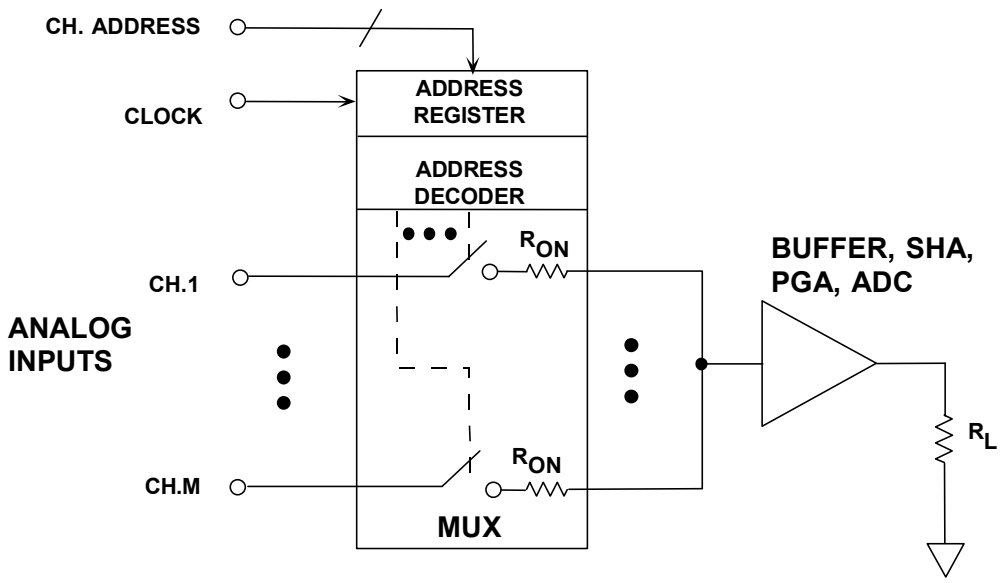
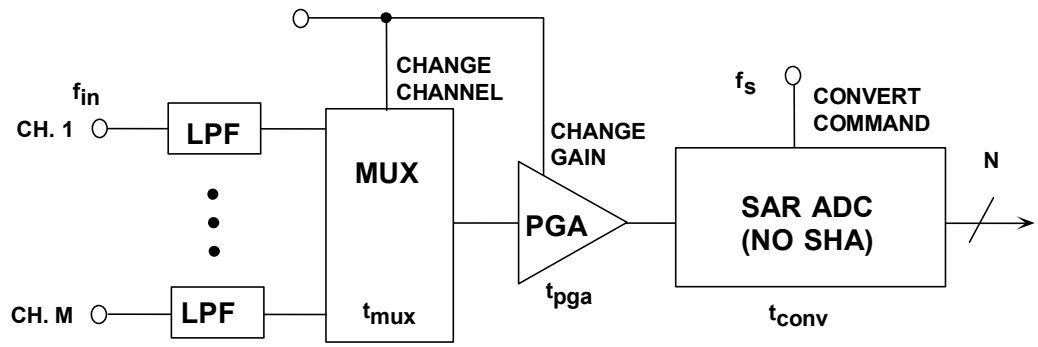


Figure 8.33: *Simplified Diagram of a Typical Analog Multiplexer*

Multiplexer on-resistance is generally slightly dependent on the signal level (often called R_{on} modulation). This will cause signal distortion if the multiplexer must drive a load resistance, therefore the multiplexer output should be isolated from the load with a suitable buffer amplifier. A separate buffer is not required if the multiplexer drives a high input impedance, such as a PGA, SHA or ADC—but beware! Some SHAs and ADCs draw high frequency pulse current at their sampling rate and cannot tolerate being driven by an unbuffered multiplexer.

An M-channel multiplexed data acquisition system is shown in Figure 8.34. The multiplexer output drives a PGA whose gain can be adjusted on a per-channel basis depending on the channel signal level. This ensures that all channels utilize the full dynamic range of the ADC. The PGA gain is changed at the same time as the multiplexer is switched to a new channel. The ADC *Convert Command* is applied after the multiplexer and the PGA have settled to the required accuracy (1 LSB). The maximum sampling frequency (when switching between channels) is limited by the multiplexer switching time t_{mux}, the PGA settling time t_{pga}, and the ADC conversion time t_{conv} as shown in the formula.



$$f_S \le \frac{1}{t_{conv} + \sqrt{t_{mux}^2 + t_{pga}^2}}$$

$$f_{in} \le \frac{1}{\pi 2^N \bullet t_{conv}}$$

Example: If N = 12 and t_{conv} = 20µsec,
Then f_{in} ≤ 4Hz!!!

Figure 8.34: *Multiplexed Data Acquisition System with PGA and SAR ADC*

In a multiplexed system it is possible to have a positive fullscale signal on one channel and a negative fullscale signal on the other. When the multiplexer switches between these channels its output is a fullscale step voltage. All elements in the signal path must settle to the required accuracy (1 LSB) before the conversion is started. The effect of inadequate settling is dc crosstalk between channels.

The SAR ADC shown in this application has no internal SHA (similar to the industry-standard AD574-series), and therefore the input signal must be held constant (within 1 LSB) during the conversion time in order to prevent encoding errors. This defines the maximum rate-of-change of the input signal:

$$\left.\frac{dv}{dt}\right|_{max} \le \frac{1LSB}{t_{conv}} \qquad \text{Eq. 8.7}$$

The amplitude of a fullscale sinewave input signal is equal to $2^N/2$, or $2^{(N-1)}$, and its maximum rate-of change is

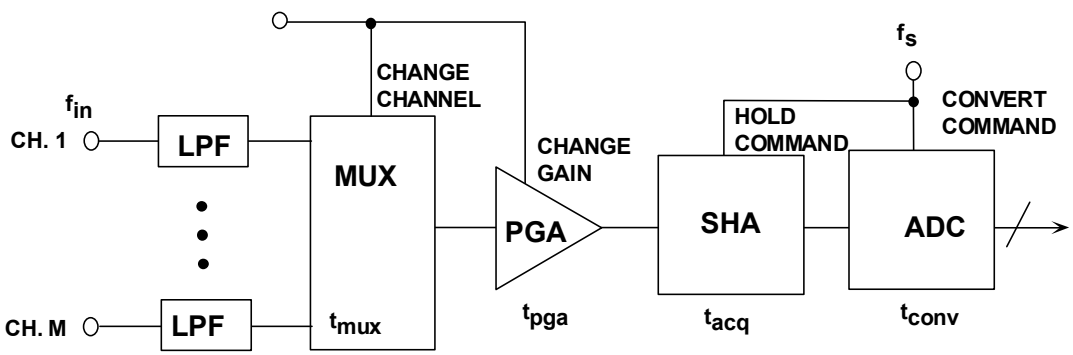
$$\left.\frac{dv}{dt}\right|_{max} = 2\pi f_{max} \cdot 2^{N-1} = \pi f_{max} \cdot 2^{N}. \qquad \text{Eq. 8.8}$$

Setting the two equations equal, and solving for f_{max},

$$f_{max} \le \frac{1}{\pi \cdot 2^{N} t_{conv}} \quad . \qquad \text{Eq. 8.9}$$

For example, if the ADC conversion time is 20 µsec (corresponding to a maximum sampling rate of slightly less than 50 kSPS, because of overhead), and the resolution is 12-bits, then the maximum channel input signal frequency is limited to 4 Hz. This may be adequate if the signals are dc, but the lack of a SHA function severely limits the ability to process dynamic signals.

Adding a SHA function to the ADC as shown in Figure 8.35 allows processing of much faster signals with almost no increase in system complexity, since the wide variety of sampling ADCs available today have the SHA function on-chip.



In General, $\sqrt{t_{mux}^2 + t_{pga}^2} \ll t_{acq} + t_{conv}$

Therefore, $f_S \le \dfrac{1}{t_{acq} + t_{conv}}$

Example: If t_{acq} = 1µsec, t_{conv} = 9µs, then $f_S \le$ 100kSPS
Then $f_{in} \le f_S/2M$

Figure 8.35: *The Addition of a SHA Function to the ADC Allows Processing of Dynamic Input Signals*

The timing is adjusted such that the multiplexer and the PGA are switched immediately following the acquisition time of the SHA as shown in Figure 8.36. If the combined multiplexer and PGA settling time is less than the ADC conversion time, then the maximum sampling frequency of the system is given by:

$$f_s \le \frac{1}{t_{acq} + t_{conv}}. \qquad \text{Eq. 8.10}$$

The per-channel sampling rate is obtained by dividing the ADC sampling rate given in Eq. 8.10 by M.

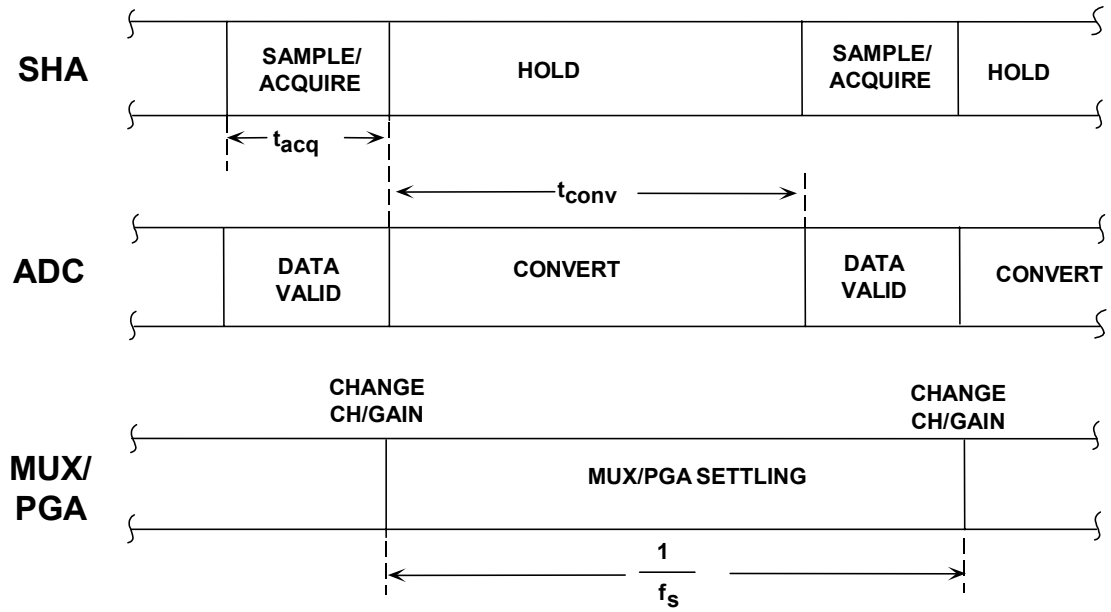
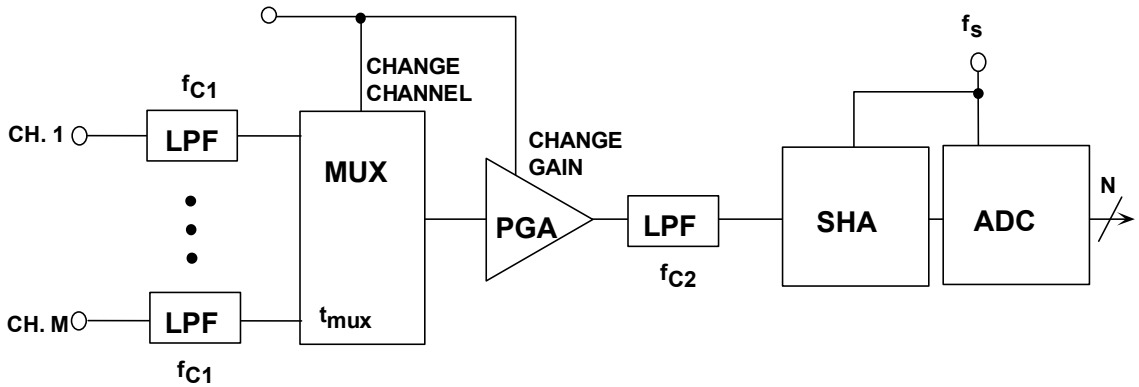


Figure 8.36: *Typical Timing Diagram for Multiplexed Data Acquisition System Using a SHA*

Filtering Considerations in Data Acquisition Systems

Filtering in data acquisition systems not only prevents aliasing of unwanted signals but also reduces noise by limiting bandwidth. In a multiplexed system, there are basically two places to put filters: in each channel, and at the multiplexer output (see Figure 8.37).



$$\text{For Sequential Sampling, } f_{C1} < \frac{f_s}{2\,M}$$

Figure 8.37: *Filtering in a Data Acquisition System*

The filter at the input of each channel is used to prevent aliasing of signals which fall outside the Nyquist bandwidth. The per-channel sampling rate (assuming each channel is sampled at the same rate) is f_S/M, and the corresponding Nyquist frequency is $f_S/2M$. The filter should provide sufficient attenuation at $f_S/2M$ to prevent dynamic range limitations due to aliasing.

A second filter can be placed in the signal path between the multiplexer output and the ADC, usually between the PGA and the SHA. The cutoff frequency of this filter must be carefully chosen because of its impact on settling time. In a multiplexed system such as shown in Figure 8.37, there can be a fullscale step voltage change at the multiplexer output when it is switched between channels. This occurs if the signal on one channel is positive fullscale, and the signal on the adjacent channel is negative fullscale. From the timing diagram shown in Figure 8.36, the signal from the filter has essentially the entire conversion period ($1/f_S$) to settle from the step voltage. The signal should settle to within 1 LSB of the final value in order not to introduce a significant error. The settling time requirement therefore places a lower limit on the filter's cutoff frequency. The single-pole filter settling time required to maintain a given accuracy is shown in Figure 8.38. The settling time requirement is expressed in terms of the filter time constant and also the ratio of the filter cutoff frequency, f_{c2},to the ADC sampling frequency, f_S.

RESOLUTION, # OF BITS	LSB (%FS)	# OF TIME CONSTANTS	f_{c2}/f_s
6	1.563	4.16	0.67
8	0.391	5.55	0.89
10	0.0977	6.93	1.11
12	0.0244	8.32	1.32
14	0.0061	9.70	1.55
16	0.00153	11.09	1.77
18	0.00038	12.48	2.00
20	0.000095	13.86	2.22
22	0.000024	15.25	2.44

Figure 8.38: *Single-Pole Filter Settling Time to Required Accuracy*

As an example, assume that the ADC is 12-bits and sampling at 100 kSPS. From the table in Figure 8.38, 8.32 time constants are required for the filter to settle to 12-bit accuracy, and

$$\frac{f_{c2}}{f_s} \geq 1.32\,, \text{ or } f_{c2} \geq 132 \text{ kSPS.} \qquad \text{Eq. 8.11}$$

While this filter will help prevent wideband noise from entering the SHA, *it does not provide the same function as the antialiasing filters at the input of each channel*.

The above analysis assumes that the multiplexer/PGA combined settling time is significantly less than the filter settling time. If this is not the case, then the filter cutoff frequency must be larger, and in most cases it should be left out entirely in favor of per-channel filters.

We have discussed the importance of the fullscale settling time of the multiplexer/PGA/filter combination, but what is equally important is the ability of the ADC to acquire the final value of the step voltage input signal to the required accuracy. Failure of any link in the signal chain to settle will result in dc crosstalk between adjacent channels and loss of accuracy. If the data acquisition system uses a separate SHA and ADC, then the key specification to examine is the SHA *acquisition time*, which is usually specified as the amount of time required to acquire a fullscale input signal to 0.1% accuracy (10-bits) or 0.01% accuracy (13-bits). In most cases, both 0.1% and 0.01% times are specified. If the SHA acquisition time is not specified for 0.01% accuracy or better, it should not be used in a 12-bit multiplexed application.

If the ADC is a sampling type (with internal SHA), the SHA acquisition time required to achieve a level of accuracy may or may not be specified. Because SHA acquisition time and accuracy are not directly specified for some sampling ADCs, the *transient response* specification should be examined. The transient response of the ADC (settling time to within 1 LSB for a fullscale step input) must be less the $1/f_S$, where f_S is the ADC sampling rate. This often ignored specification may become the weakest link in the signal chain. In some cases neither the SHA acquisition time to specified accuracy nor the transient response specification appear on the data sheet for the particular ADC, in which case it is probably not acceptable for multiplexed applications. Because of the difficulty in measuring and achieving better than 12-bit settling times using discrete components, the accuracy of most multiplexed data acquisition systems made up of discrete components is limited to 14-bits at best. Designing multiplexed systems with greater accuracy is extremely difficult, and using a single ADC per channel should be strongly considered at higher resolutions. The modern alternative, of course, is to use an ADC with an on-chip multiplexer where the overall performance of the combination is specified.

Complete Data Acquisition Systems on a Chip

VLSI mixed-signal CMOS processing allows the integration of large and complex data acquisition circuits on a single chip. Most signal conditioning circuits including multiplexers, PGAs, and SHAs, are now integrated onto the same chip as the ADC. This high level of integration permits data acquisition systems to be specified and tested as a single complex function.

Such functionality relieves the designer of most of the burden of testing and calculating individual component error budgets. The dc and ac characteristics of a complete data acquisition system are specified as a complete function, which removes the necessity of calculating performance from a collection of individual worst case device specifications. A complete monolithic system should achieve a higher performance at much lower cost than would be possible with a system built up from discrete functions. Furthermore, system calibration is easier and in fact many monolithic systems are self calibrating.

With these high levels of integration, it is both easy and inexpensive to make many of the parameters of the device programmable. Parameters which can be programmed include gain, filter cutoff frequency, and even ADC resolution and conversion time, as well as the obvious digital/MUX functions of input channel selection, output data format, and range selection.

The *data acquisition system on a chip* concept has led to the proliferation of so many ICs, that it would be impossible to discuss all of them in detail. We will, however, discuss a few of the newer devices which are representative of the entire family. All are completely specified in terms of both dc and ac performance, and many come in 8-, 10-, and 12-bit versions.

The AD7908/AD7918/AD7928 are, respectively, 8-bit, 10-bit, and 12-bit, high speed, low power, 8-channel, successive approximation ADCs. The parts operate from a single 2.7-V to 5.25-V power supply and feature throughput rates up to 1 MSPS. The parts contain a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 8 MHz. A block diagram of the AD7908/AD7918/AD7928 is shown in Figure 8.39.

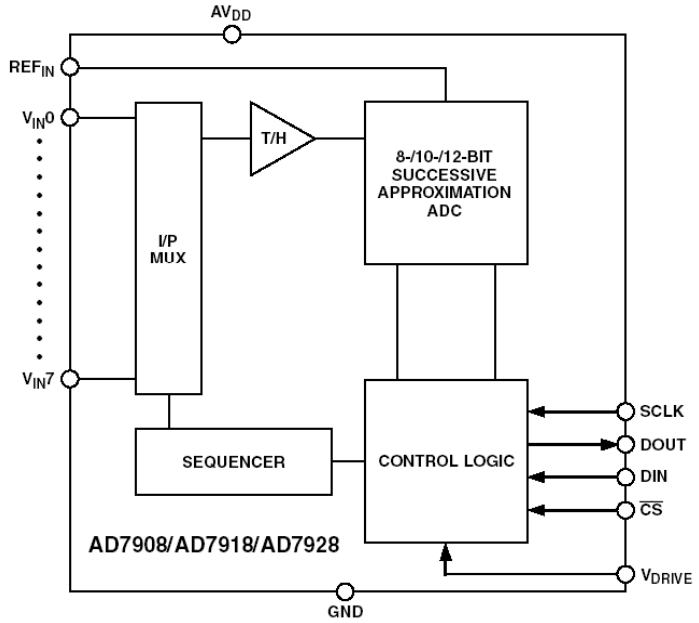


Figure 8.39: *AD7908/AD7918/AD7928 8-Channel, 1-MSPS 8-/10-/12-Bit SAR ADCs with Channel Sequencer*

The conversion process and data acquisition are controlled using $\overline{CS}$ (convert start) and the serial clock signal (nominally SCLK = 20 MHz), allowing the device to easily interface with microprocessors or DSPs via a serial interface. The input signal is sampled on the falling edge of $\overline{CS}$, and conversion is also initiated at this point. There are no pipeline delays associated with the part.

The AD7908/AD7918/AD7928 use advanced design techniques to achieve very low power dissipation at maximum throughput rates. At maximum throughput rates, the

AD7908/AD7918/AD7928 consume 2-mA maximum with 3-V supplies; with 5-V supplies, the current consumption is 2.7-mA maximum.

Through the configuration of the Control Register, the analog input range for the part can be selected as 0 V to REF_{IN} or 0 V to $2 \times REF_{IN}$, with either straight binary or twos complement output coding. The AD7908/AD7918/AD7928 each feature eight single-ended analog inputs with a channel sequencer to allow a preprogrammed selection of channels to be converted sequentially. The conversion time for the AD7908/AD7918/AD7928 is determined by the SCLK frequency, which is also used as the master clock to control the conversion. The maximum throughput rate is 1 MSPS using a serial clock frequency of 20 MHz. The devices are available in a 20-lead TSSOP package.

The AD7938/AD7939 are 12- and 10-bit, high speed, low power, successive approximation (SAR) ADCs which supply a parallel data output. A simplified block diagram is shown in Figure 8.40. The parts operate from a single 2.7-V to 5.25-V power supply and feature throughput rates up to 1.5 MSPS. The parts contain a low noise, wide bandwidth, differential track/hold amplifier that can handle input frequencies up to 20 MHz.

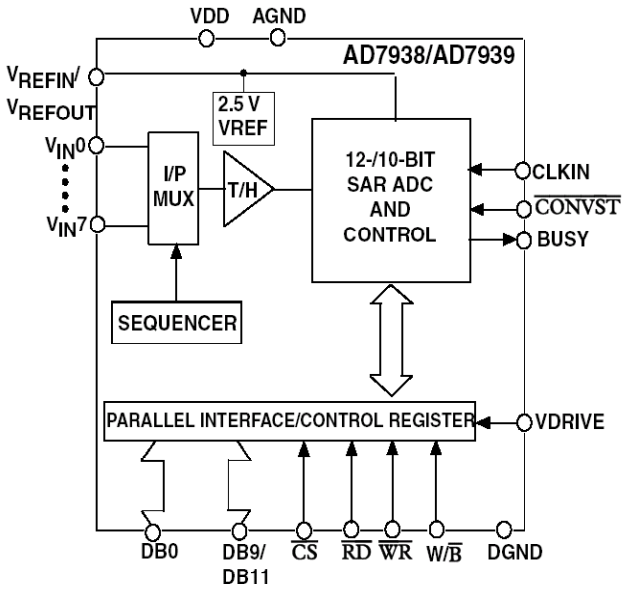


Figure 8.40: *AD7938/AD7939 8-Channel, 1.5-MSPS 12-/10-Bit Parallel Output ADC with Sequencer*

The AD7938/AD7939 feature 8 analog input channels with a channel sequencer to allow a pre-programmed selection of channels to be converted sequentially. These parts can operate with either single-ended, fully differential or pseudo-differential analog inputs. The analog input configuration is chosen by setting the relevant bits in the on-chip Control Register.

The conversion process and data acquisition are controlled using standard control inputs allowing easy interfacing to Microprocessors and DSPs. The input signal is sampled on the falling edge of $\overline{CONVST}$, and the conversion is also initiated at this point.

The AD7938/AD7939 has an accurate on-chip 2.5-V reference that can be used as the reference source for the analog to digital conversion. Alternatively, this pin can be overridden to provide an external reference in the range 100 mV to 3.5 V. See the AD7938/AD7939 data sheet for performance when using various external reference voltage values.

These parts use advanced design techniques to achieve very low power dissipation at high throughput rates. They also feature flexible power management options. An on-chip Control Register allows the user to set up different operating conditions including analog input range and configuration, output coding, power management, and channel sequencing. The parts are available in a 32-pin LFCSP package.

Multiplexing Inputs to Σ-Δ ADCs

As was discussed in Chapter 3, the digital filter is an integral part of a Σ-Δ ADC. When the input to a Σ-Δ ADC changes by a large step, the entire digital filter must fill with the new data before the output becomes valid, which is a slow process. This is why Σ-Δ ADCs are sometimes said to be unsuitable for multi-channel multiplexed systems—they are not inherently so, but the time taken to change channels can be inconvenient. Generally speaking, the settling time is on the order of several clock cycles of the output data rate.

However, it is possible to optimize the digital filter and the rest of the Σ-Δ ADC design to yield high throughputs in multiplexed applications. For example, the AD7739 (Reference 3) is an 8-channel input high precision, high throughput Σ-Δ ADC optimized for multiplexed applications. A simplified block diagram is shown in Figure 8.41.

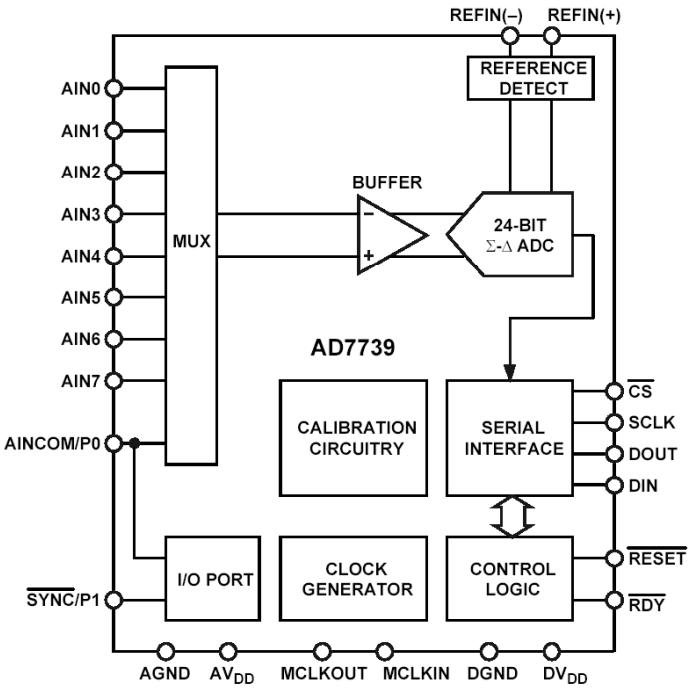


Figure 8.41: *AD7739 8-Channel, High Throughput,24-Bit Σ-Δ ADC*

The AD7739 has true 16-bit noise-free code resolution with a total conversion time of 250 µs (4-kHz channel switching), making it ideally suited to high resolution multiplexing applications.

The part can be configured via a simple digital interface, which allows users to balance the noise performance against data throughput up to 15 kHz. The analog front end features eight single-ended or four fully differential input channels with unipolar or bipolar 625-mV, 1.25-V, and 2.5-V input ranges. It accepts a common-mode input voltage from 200-mV above AGND to AVDD – 300 mV. The differential reference input features "No-Reference" detect capability. The ADC also supports per-channel system calibration options.

The digital serial interface can be configured for 3-wire operation and is compatible with microcontrollers and digital signal processors. All interface inputs are Schmitt triggered. The part is specified for operation over the extended industrial temperature range of –40°C to +105°C. Other parts in the AD7739 family are the AD7738, AD7734, and AD7732. The AD7738 is similar to the AD7739 but has higher speed (8.5-kHz channel switching for 16-bit performance) and higher AIN leakage current.

The AD7738 multiplexer output is pinned out externally, allowing the user to implement programmable gain or signal conditioning before being applied to the ADC. The AD7734 ADC features four single-ended input channels with unipolar or true bipolar input ranges to ±10 V while operating from a single +5-V analog supply. The AD7734 accepts an analog input overvoltage to ±16.5 V without degrading the performance of the adjacent channels. The AD7732 is similar to the AD7734, but its analog front end features two fully differential input channels.

The specified conversion time includes one or two settling and sampling periods and a scaling time as shown in Figure 8.42. With chopping enabled, a conversion cycle starts with a settling time of 43 or 44 MCLK cycles (~7.1 µs with a 6.144-MHz MCLK) to allow the circuits following the multiplexer to settle. The Σ-Δ modulator constantly samples the analog signals, and the digital filter processes the digital data stream. The sampling time depends on the channel conversion time register contents. For the example shown, the sampling time is 105.3 µs.

After another settling time of 42 MCLK cycles (~6.8 µs), the sampling time is repeated with a reversed (chopped) analog input signal. Then, during the scaling time of 163 MCLK cycles (~26.5 µs), the two results from the digital filter are averaged, scaled using the calibration registers, and written into the channel data register.

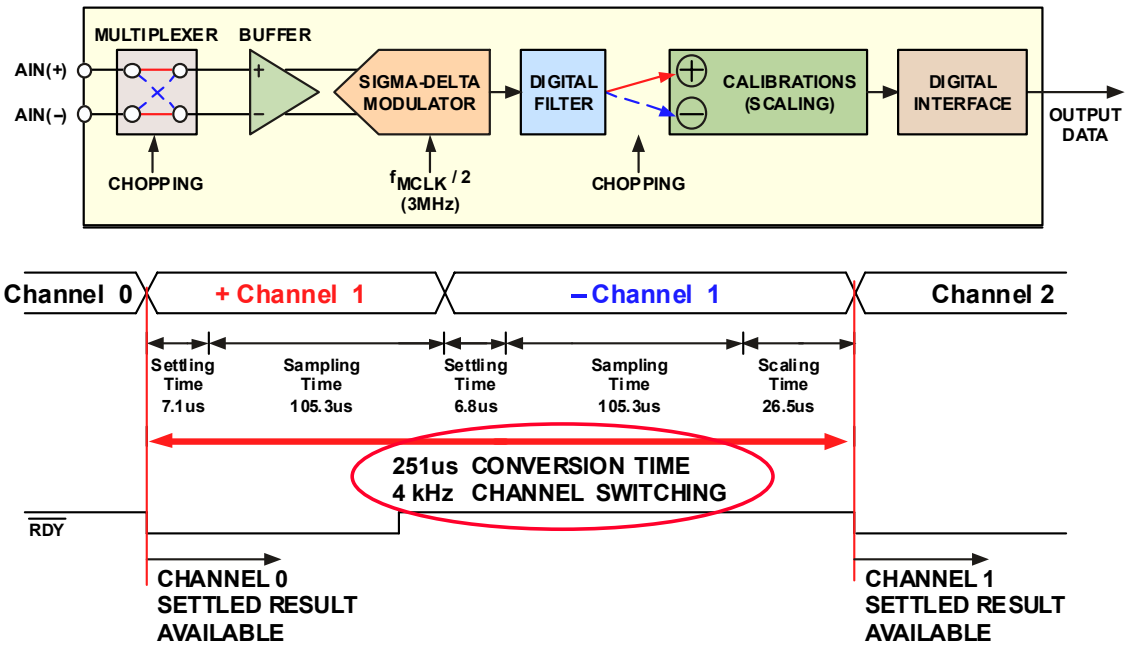


Figure 8.42: *AD7739 Timing Showing Channel Switching*

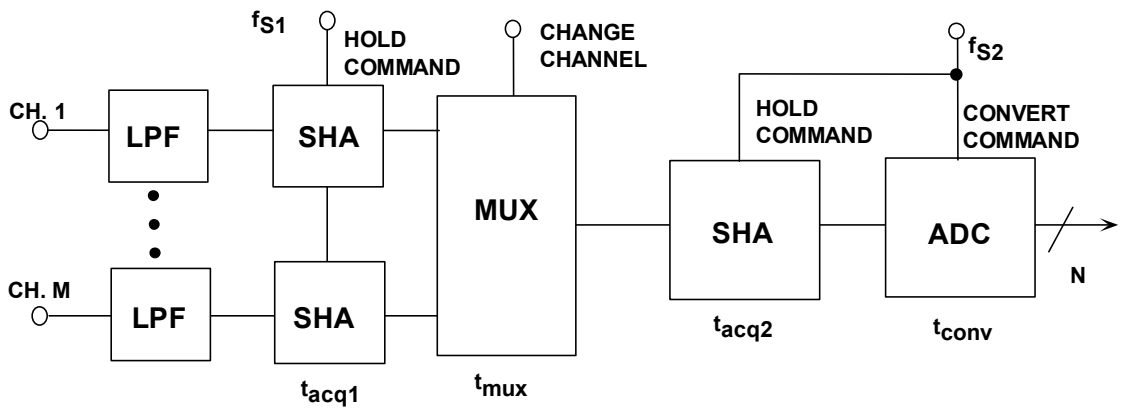
Simultaneous Sampling Systems

There are certain applications where it is desirable to sample a number of channels simultaneously such as in-phase and quadrature (I and Q) signal processing. A typical configuration is shown in Figure 8.43. Each channel requires its own filter and SHA. Each SHA is simultaneously placed in the *hold* mode by a common command signal. During the input SHAs' hold time the multiplexer is sequentially switched from channel to channel, and the sampling ADC is used to digitize the signal on each channel. The acquisition time of the second SHA, t_{acq2}, must be considered in determining the maximum ADC sampling rate, f_{s2}. The multiplexer should be switched to the next channel after the single SHA goes into the hold mode. If the multiplexer settling time is less than the ADC conversion time, then the maximum ADC sampling rate f_{s2} is the reciprocal of the sum of the SHA acquisition time and the ADC conversion time.

$$f_{s2} \leq \frac{1}{t_{acq2} + t_{conv}}. \qquad \text{Eq. 8.12}$$

The maximum input sampling frequency is less than this value divided by M, where M is the number of channels. Additional timing overhead (t_{acq1}) is required for the simultaneous SHAs to acquire the signals.

$$f_{s1} < \frac{1}{t_{acq1} + M(t_{conv} + t_{acq2})}. \qquad \text{Eq. 8.13}$$



$$f_{S2} \le \frac{1}{t_{acq2} + t_{conv}}$$

$$f_{S1} \le \frac{1}{t_{acq1} + M(t_{acq2} + t_{conv})} = \frac{1}{t_{acq1} + \frac{M}{f_{S2}}}$$

Assuming $t_{mux} < t_{acq2} + t_{conv}$

Figure 8.43: *Simultaneous Sampling Data Acquisition System Using Sampling ADC*

The AD7865 is a fast, low power, four-channel simultaneous sampling 14-bit SAR ADC that operates from a single 5-V supply (Reference 4). The part contains a 2.4-µs successive approximation ADC, four track/hold amplifiers, 2.5-V reference, on-chip clock oscillator, signal conditioning circuitry and a high speed parallel interface. A simplified block diagram of the AD7865 is shown in Figure 8.44.

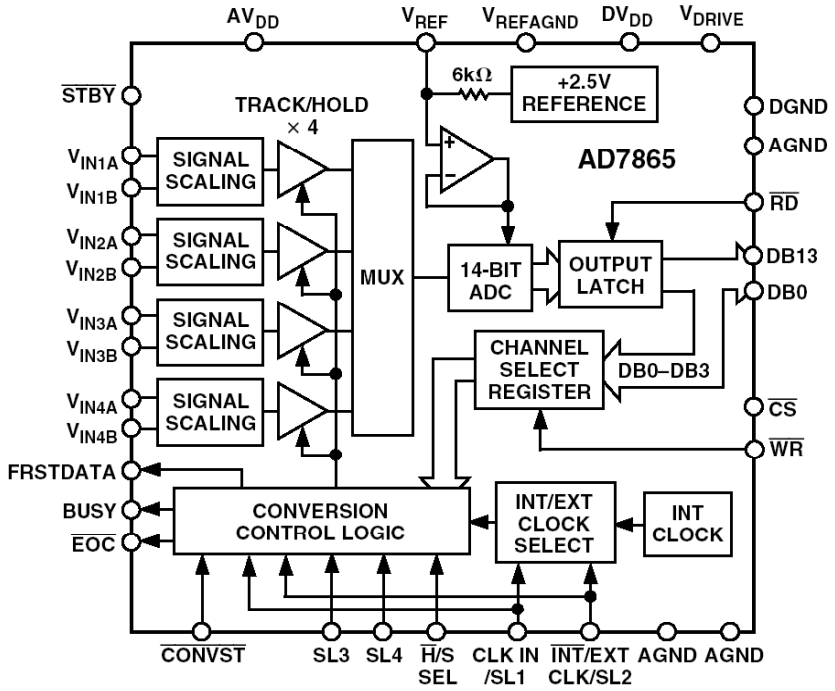


Figure 8.44: *AD7865 4-Channel Simultaneous Sampling 14-Bit SAR ADC*

The input signals on four channels are sampled simultaneously, thus preserving the relative phase information of the signals on the four analog inputs. Aperture delay matching between the sample-and-holds is less than 4 ns. The part accepts analog input ranges of ±10 V, ±5 V, ±2.5 V, 0 V to +2.5 V and 0 V to +5 V. The part allows any subset of the four channels to be converted in order to maximize the throughput rate on the selected sequence. The channels to be converted can be selected either via hardware (channel select input pins) or via software (programming the channel select register).

A single conversion start signal ($\overline{\text{CONVST}}$) simultaneously places all the track/holds into hold and initiates conversion sequence for the selected channels. The $\overline{\text{EOC}}$ signal indicates the end of each individual conversion in the selected conversion sequence. The BUSY signal indicates the end of the conversion sequence. Data is read from the part via a 14-bit parallel data bus using the standard $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals. Maximum throughput for a single channel is 350 kSPS. For all four channels the maximum throughput is 100 kSPS. The AD7865 is available in a 44-lead PQFP.

In simultaneous sampling applications using one Σ-Δ ADC per channel, the outputs must be synchronized as shown in Figure 8.45. Although the inputs are sampled at the same instant at a rate Kf_S, the decimated output frequency, f_S, is generally derived internally in each ADC by dividing the input sampling frequency by K (the oversampling rate) as shown in Figure 8.44. The output data must therefore be synchronized by the same clock at a frequency f_S. Most Σ-Δ ADCs provide a SYNC input to allow this synchronization.

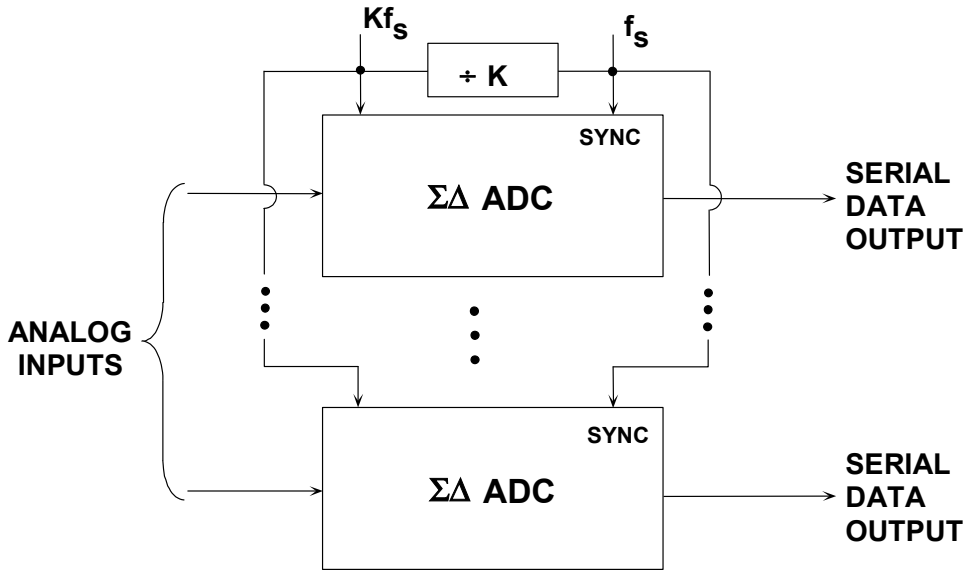


Figure 8.45: *Synchronizing Σ-Δ ADCs in Simultaneous Sampling Applications*

Data Distribution Systems

In many industrial and process control applications, multiple programmable voltage sources are required. Traditionally, these applications have required a large number of components, but recent product developments have greatly reduced the parts count without compromising performance.

Multiple voltage outputs can either be derived by demultiplexing the output of a single DAC or by employing multiple DACs. These two approaches are shown in Figure 8.46. In the demultiplexed circuit (A), one DAC feeds the inputs of several sample-and-hold amplifiers (SHA). The equivalent digital value for the analog output is applied to the DAC, and the appropriate SHA is selected. After the DAC settling time and SHA acquisition time requirements have been met, the SHA can be deselected and the next channel updated. Once a SHA is deselected, the output voltage will begin to droop at a rate specified for the SHA. Thus, the SHA must be refreshed before the output voltage droop exceeds the required accuracy (typically ½ LSB).

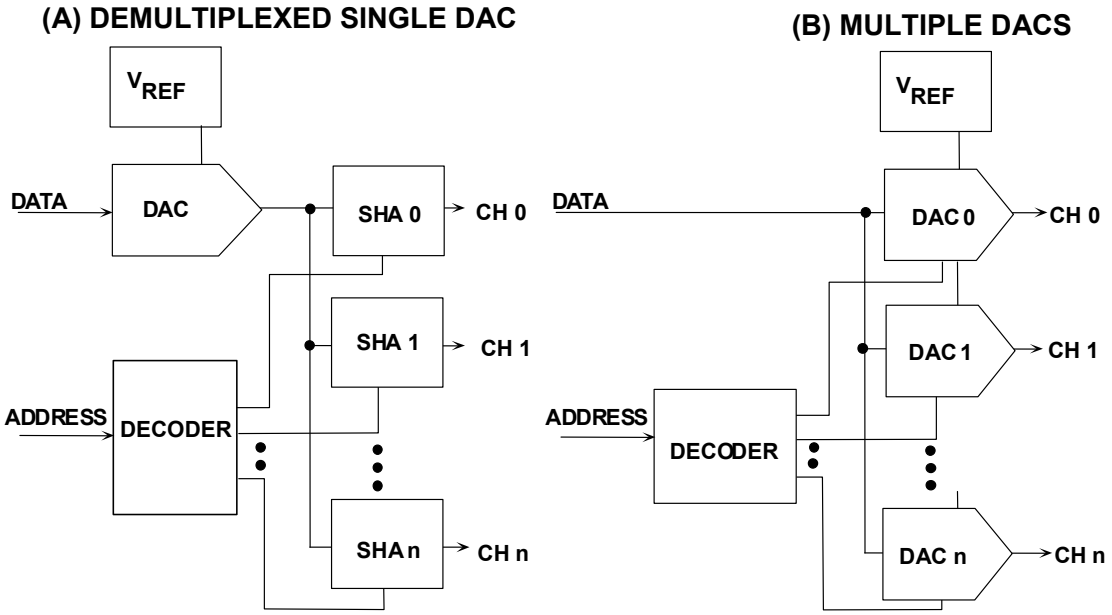


Figure 8.46: *Options for Analog Data Distribution*

The DAC plus SHA system evolved because, in the past, DACs were more expensive than SHAs. This situation was particularly true for DACs with resolution above 8 bits. In addition, multiple-SHAs with on-chip hold capacitors reduced the parts count, printed circuit board area, and cost of demultiplexed DAC systems. Finally, the demultiplexed DAC only required one calibration step, since the same DAC provides the output voltage for each of the output channels. Of course, single-calibration is only valid if the SHA does not introduce unacceptable errors.

Today, however, the DAC plus SHA approach is virtually obsolete because of the availability of high resolution, low cost integrated circuit DACs in duals, quads, octals, etc. The multiple DAC application shown in Figure 8.46B is straightforward. One DAC

is provided for each channel, and an address decoder simply selects the appropriate DAC. No refresh is required.

There is a high demand not only for multiple DACs in a single package, but also for single DACs in small low cost low power packages. Figure 8.47 shows two methods for distributing data to several remote locations. The method shown in Figure 8.47A uses multiple DACs to distribute analog data to multiple remote locations. This method requires that the analog signals be protected from noise pickup, and requires the use of shielded cables. If the remote stages are located a long distance from the source, then the method of Figure 8.47B is preferred, where the digital data is transmitted over the remote cable link, and individual DACs are used as each of the remote stages.

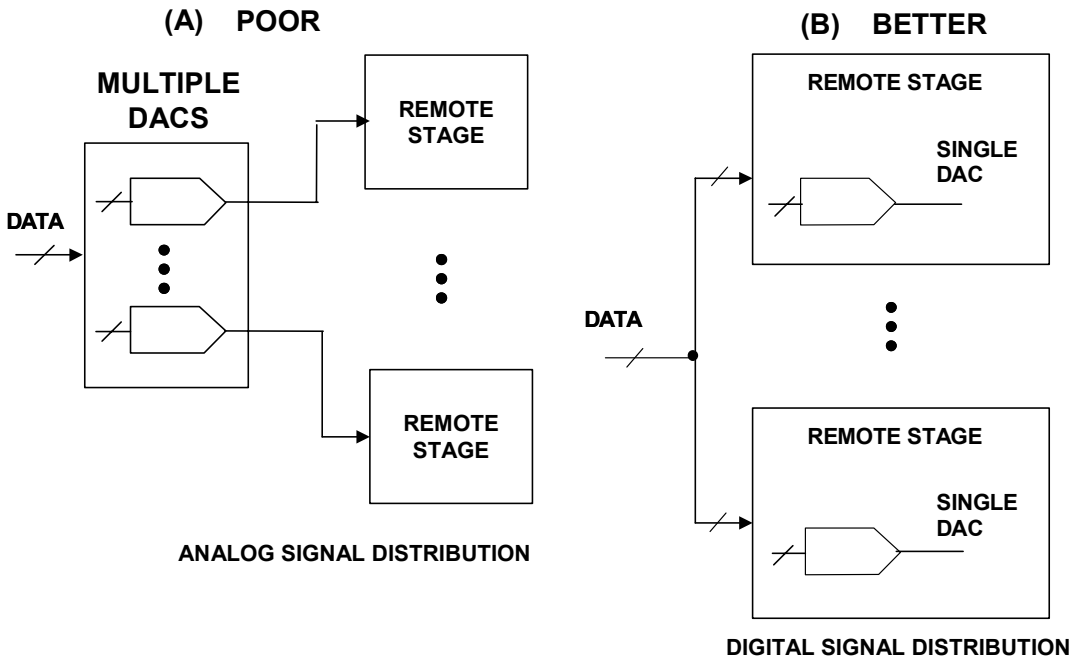


Figure 8.47: *Remote, Multichannel Data Distribution*

An excellent example of a low cost single DAC is the AD5320 12-bit buffered voltage output DAC (Reference 5). A simplified block diagram is shown in Figure 8.48. AD5320 is one of a family of pin-compatible DACs. The AD5300 is the 8-bit version and the AD5310 is the 10-bit version. The AD5300/AD5310/AD5320 are available in 6-lead SOT-23 packages and 8-lead µSOIC packages.

The AD5320 operates from a single +2.7-V to +5.5-V supply consuming 115 µA at 3 V. Its on-chip precision output amplifier allows rail-to-rail output swing to be achieved. The AD5320 utilizes a versatile three-wire serial interface that operates at clock rates up to 30 MHz and is compatible with standard SPI®, QSPI®, MICROWIRE® and DSP interface standards. The reference for AD5320 is derived from the power supply inputs and thus gives the widest dynamic output range.

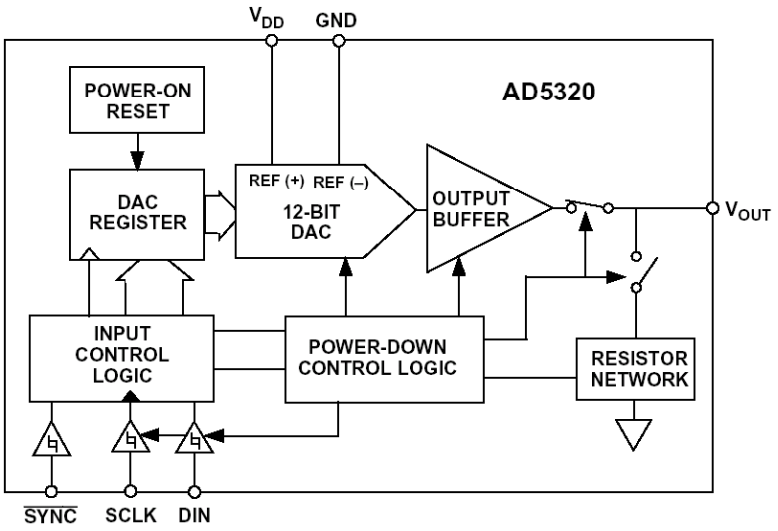


Figure 8.48: *AD5320 12-Bit Serial Input DAC in SOT-23 6-Pin Package*

The part incorporates a power-on reset circuit that ensures that the DAC output powers up to zero volts and remains there until a valid write takes place to the device. The part contains a power-down feature that reduces the current consumption of the device to 200 nA at 5 V and provides software selectable output loads while in power-down mode. The part is put into power-down mode over the serial interface. The low power consumption of this part in normal operation makes it ideally suited to portable battery operated equipment. The power consumption is 0.7 mW at 5 V reducing to 1 µW in power-down mode.

There are many other single DACs in small packages with and without on-chip references. Resolutions range from 8- to 16-bits. Selection guides are helpful in selecting the right one for a particular application. One of the newer parts is the AD5660 16-Bit serial input DAC with a 10-ppm/°C on-chip voltage reference (Reference 6). This device is available in an 8-lead SOT-23 package and operates on a supply voltage of +2.7 V to +5.5 V.

For operation at higher supply voltages, the AD5570 (Reference 7) is a single 16-bit serial input, voltage output DAC that operates from supply voltages of ±12 V up to ±15 V. INL and DNL are accurate to 1-LSB (max) over the full temperature range of –40°C to +125°C. The AD5570 utilizes a versatile three-wire interface. The AD5570 is available in a 16-pin SSOP package.

For localized distribution of multiple analog signals, dual, quad, octal, etc., DACs are generally much preferred to single DACs. Multiple DACs find applications in instrumentation, process control, ATE, and many other applications. These DACs are generally double-buffered so that data can be loaded via a serial port and then the actual internal parallel DAC register updated either simultaneously or individually. Again, these DACs are available in many resolutions, voltage/current ranges, supply voltage, packages, etc., so a complete discussion of all options is impossible here. We will look at a couple of newer offerings as examples.

The AD5516 consists of sixteen 12-bit DACs in a single package (Reference 8). A functional block diagram is shown in Figure 8.49. A single reference input pin (REF_IN) is used to provide a 3 V reference for all 16 DACs. To update a DAC's output voltage, the required DAC is addressed via the 3-wire serial interface. Once the serial write is complete, the selected DAC converts the code into an output voltage. The output amplifiers translate the DAC output range to give the appropriate voltage range (±2.5 V, ±5 V, or ±10 V) at output pins $V_{OUT}0$ to $V_{OUT}15$. The AD5516 uses a self-calibrating architecture to achieve 12-bit performance. The calibration routine servos to select the appropriate voltage level on an internal 14-bit resolution. The AD5516 is available a 74-lead CSPBGA package with a body size of 12 mm × 12 mm.

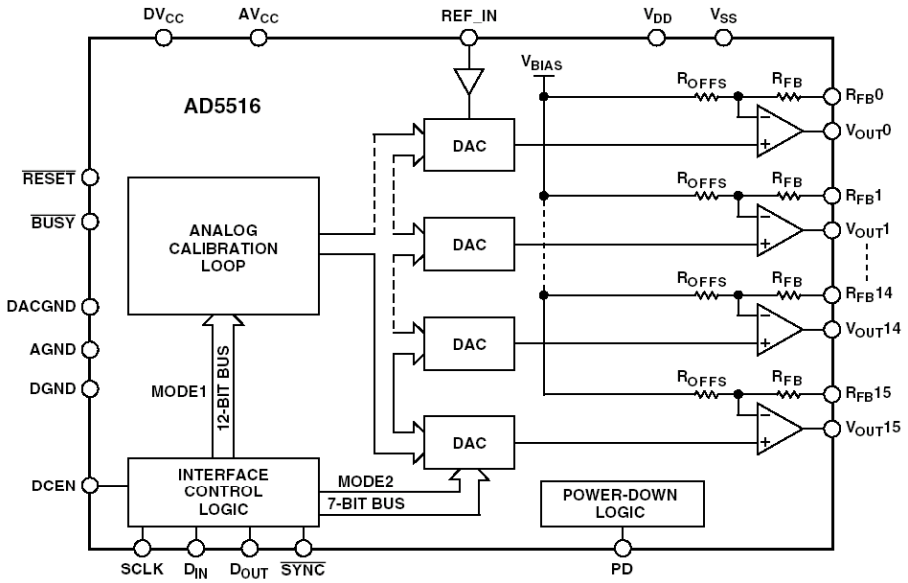


Figure 8.49: *AD5516 16-Channel 12-Bit Voltage Output DAC*

For the maximum available channel count today, the AD5379 contains forty 14-bit DACs in 13mm × 13 mm 108-lead LFBGA package and is ideal for high-end level setting needs in automatic test equipment and in optical networking applications (Reference 9). It has both parallel and 3-wire serial interfaces. A simplified block diagram is shown in Figure 8.50.

The AD5379 has a maximum output voltage span of 17.5 V which corresponds to an output range of –8.75 V to +8.75 V derived from reference voltages of –3.5 V and +5 V. The AD5379 contains a double-buffered parallel interface in which 14 data bits are loaded into one of the input registers under the control of the $\overline{WR}$, $\overline{CS}$ and DAC channel address pins, A0–A7. It also has a 3-wire serial interface which is compatible with SPI®, QSPI®, MICROWIRE® and DSP interface standards and can handle clock speeds of up to 50 MHz. The DAC outputs are updated on reception of new data into the DAC registers. All the outputs can be updated simultaneously by taking the $\overline{LDAC}$ input low. Each channel has a programmable gain and offset adjust register. Each DAC output is gained and buffered on-chip with respect to an external REFGND input. The DAC outputs can also be switched to REFGND via the $\overline{CLR}$ pin.

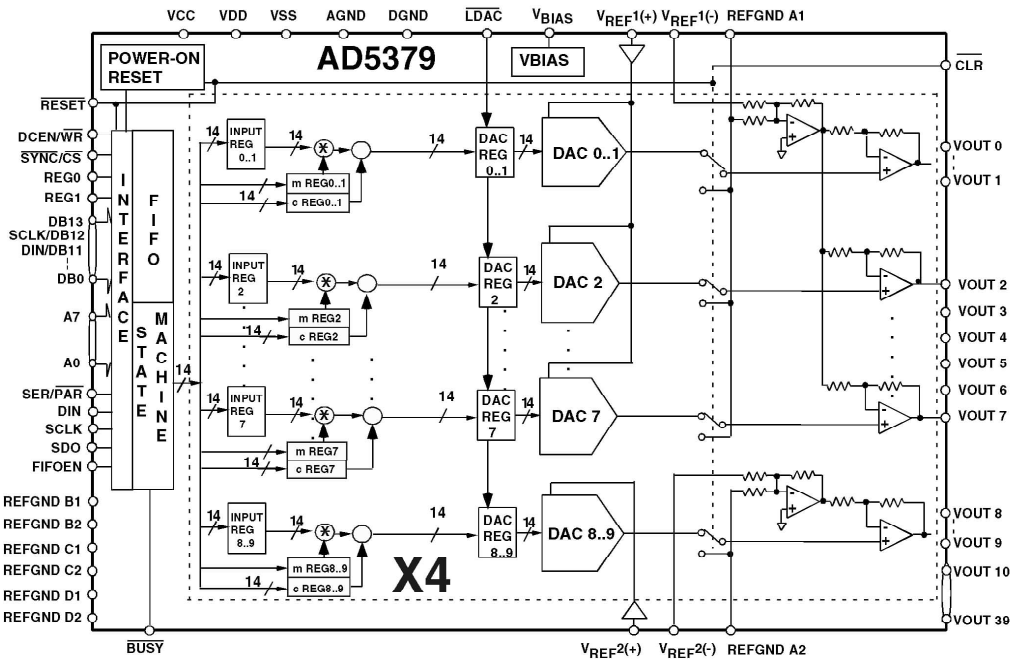


Figure 8.50: *AD5379 40-Channel, 14-Bit, Parallel and Serial Input, Voltage-Output DAC*

Data Distribution Using an Infinite Sample-and-Hold

An "infinite," or "droopless" sample-and-hold function can be obtained using an ADC and a DAC. For example, the AD5533B 32-channel "infinite sample-and-hold" can be thought of as consisting of an ADC and 32 DACs in a single package (Reference 10). A functional diagram is shown in Figure 8.51. The input voltage V_{IN} is sampled and converted into a digital word. The digital result is loaded into one of the DAC registers and is converted (with gain and offset) into an analog output voltage ($V_{OUT}0$-$V_{OUT}31$). Since the channel output voltage is effectively the output of a DAC, there is no droop associated with it. As long as power to the device is maintained, the output voltage will remain constant until this channel is addressed again.

To update a single channel's output voltage, the required new voltage level is set up on the common input pin, V_{IN}. The desired channel is then addressed via the parallel port or the serial port. When the channel address has been loaded, provided $\overline{TRACK}$ is high, the circuit begins to acquire the correct code to load to the DAC so that the DAC output matches the voltage on V_{IN}. The $\overline{BUSY}$ pin goes low and remains so until the acquisition is complete. The noninverting input to the output buffer is tied to V_{IN} during the acquisition period to avoid spurious outputs while the DAC acquires the correct code. The acquisition is completed in 16-µs max.

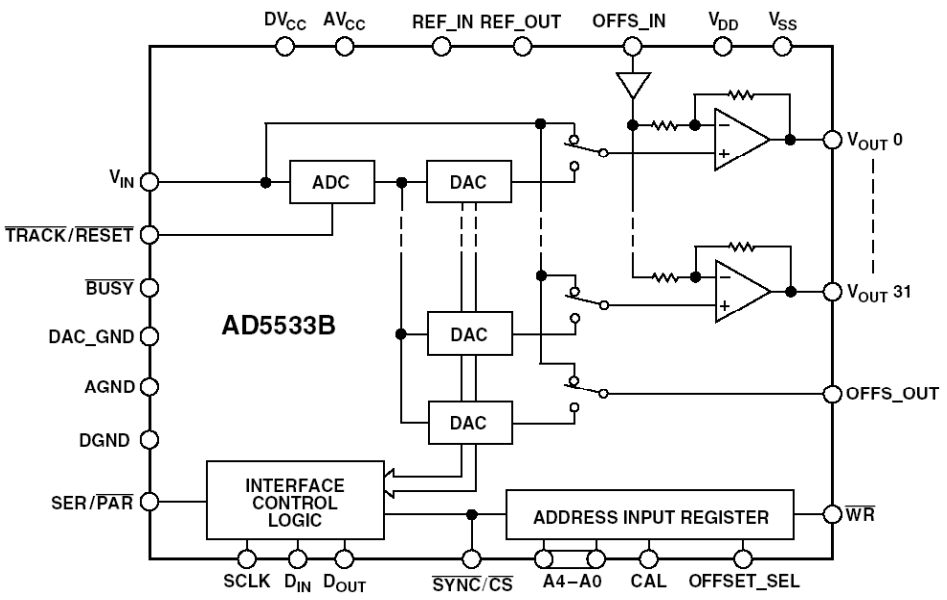


Figure 8.51: *AD5533B 32-Channel Precision Infinite Sample-and-Hold*

The $\overline{\text{BUSY}}$ pin goes high and the updated DAC output assumes control of the output voltage. The output voltage of the DAC is connected to the noninverting input of the output buffer. Since the internal DACs are offset by 70-mV (max) from GND, the minimum V_{IN} in infinite SHA mode is 70 mV. The maximum V_{IN} is 2.96 V, due to the upper dead band of 40-mV (max). On power-on, all the DACs, including the offset channel, are loaded with zeros. Each of the 32 DACs is offset internally by 50-mV (typ) from GND so the outputs $V_{OUT}0$ to $V_{OUT}31$ are 50-mV (typ) on power-on if the OFFS_IN pin is driven directly by the on-board offset channel (OFFS_OUT), i.e., if OFFS_IN = OFFS_OUT = 50 mV = > $V_{OUT} = (\text{Gain} \times V_{DAC}) - (\text{Gain} - 1) \times V_{OFFS_IN} = 50$ mV.

The output voltage range is determined by the offset voltage at the OFFS_IN pin and the gain of the output amplifier. It is restricted to a range from V_{SS} + 2 V to V_{DD} – 2 V because of the headroom of the output amplifier.

The AD5533B is operated with AV_{CC} = +5 V ± 5%, DV_{CC} = +2.7 V to +5.25 V, V_{SS} = –4.75 V to –16.5 V, and V_{DD} = +8 V to +16.5 V, and requires a stable 3-V reference on REF_IN as well as an offset voltage on OFFS_IN.

The AD5533B infinite sample-and-hold is ideally suited for use in automatic test equipment. Several ISHAs are required to control pin drivers, comparators, active loads, and signal timing as shown in Figure 8.52. Traditionally, sample-and-hold devices with droop were used in these applications. These required refreshing to prevent the voltage from drifting. The AD5533B has several advantages: no refreshing is required, there is no droop, pedestal error is eliminated, and there is no need for extra filtering to remove glitches. Overall, a higher level of integration is achieved in a smaller area.

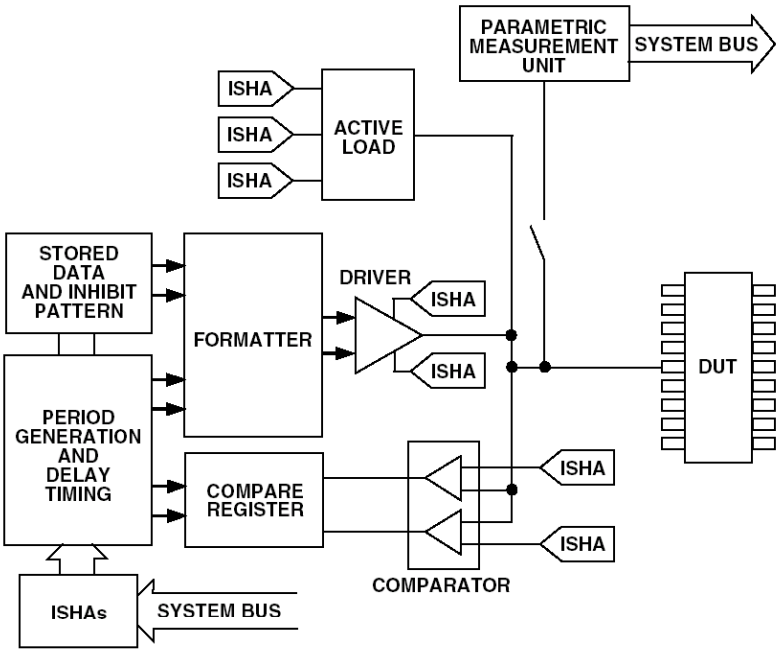


Figure 8.52: *Infinite Sample-and-Holds (ISHAs) Used in Automatic Test Equipment Systems*

The AD5533B can be used to set up voltage levels on 32 channels as shown in Figure 8.53. An AD780 provides the 3-V reference for the AD5533B, and for the AD5541 16-bit DAC. A simple 3-wire serial interface is used to write to the AD5541. Because the AD5541 has an output resistance of 6.25 kΩ (typ), the time taken to charge/ discharge the capacitance at the V_{IN} pin is significant. Thus an AD820 is therefore used to buffer the DAC output. Note that it is important to minimize noise on V_{IN} and REFIN when laying out this circuit.

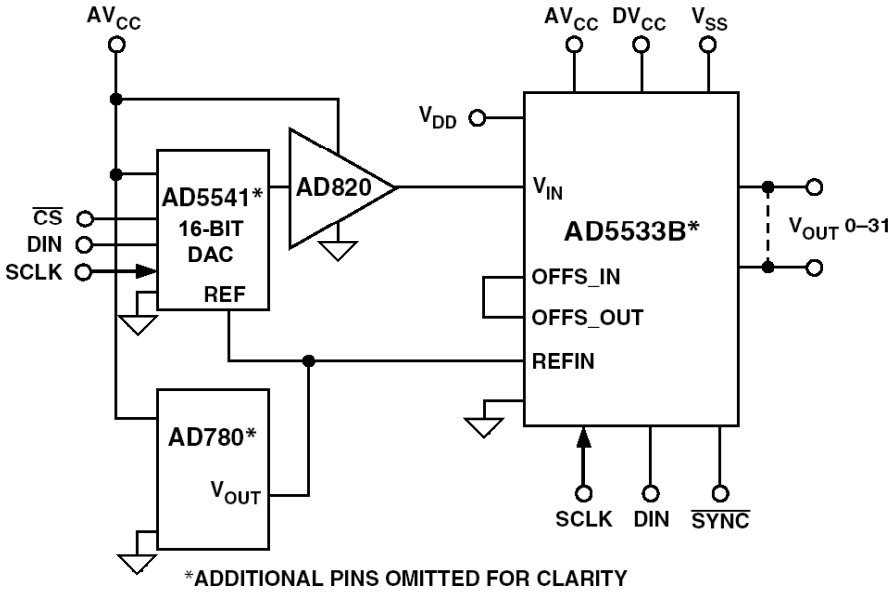


Figure 8.53: *AD5533B Infinite Sample-and-Hold Typical Application Circuit*

REFERENCES:
8.2 MULTICHANNEL DATA ACQUISITION SYSTEMS

1. Data sheet for AD7908/AD7918/AD7928 8-Channel, 1 MSPS 8-/10-/12-Bit ADCs with Sequencer in 20-Lead TSSOP, http://www.analog.com.

2. Data sheet for AD7938/AD7939 8-Channel, 1.5MSPS, 12- and 10-Bit Parallel Output ADCs with a Sequencer, http://www.analog.com.

3. Data sheet for AD7739 8-Channel, High Throughput, 24-Bit Σ-Δ ADC, http://www.analog.com.

4. Data sheet for AD7865 AD7865 4-Channel Simultaneous Sampling 14-Bit SAR ADC, http://www.analog.com.

5. Data sheet for AD5320 +2.7 V to +5.5 V, 140 µA, Rail-to-Rail Output 12-Bit DAC in a SOT-23, http://www.analog.com.

6. Data sheet for AD5660 16-Bit DAC with 10ppm/°C Max On-Chip Reference, http://www.analog.com.

7. Data sheet for AD5570 12-V/15-V, Serial Input, Voltage Output, 16-Bit DAC, http://www.analog.com.

8. Data sheet for AD5516 16-Channel, 12-Bit Voltage-Output DAC with 14-Bit Increment Mode, http://www.analog.com.

9. Data sheet for AD5379 40-Channel, 14-Bit, Parallel and Serial Input, Voltage-Output DAC, http://www.analog.com.

10. Data sheet for AD5533B 32-Channel Precision Infinite Sample-and-Hold, http://www.analog.com.

SECTION 8.3: DIGITAL POTENTIOMETERS

Walt Kester, Walt Heinzer

Introduction

Mechanical potentiometers have been used since the earliest days of electronics and provide a convenient method for the adjustment of the output of various sensors, power supplies, or virtually any device that requires some type of calibration. Timing, frequency, contrast, brightness, gain, and offset adjustments are just a few of the possibilities. However, mechanical pots have always suffered from numerous problems including physical size, mechanical wearout, wiper contamination, resistance drift, sensitivity to vibration, temperature, humidity, the need for screwdriver access, layout inflexibility, etc.

Digital potentiometers avoid all the inherent problems associated with mechanical potentiometers and are ideal replacements in new designs where there is either a microcontroller or another digital device to provide the necessary control signals. Manually controlled digital potentiometers are also available for those who do not have any on-board microcontrollers. Unlike mechanical pots, digital pots can be controlled dynamically in active control applications.

The digital potentiometer is based on the CMOS "String DAC" architecture previously described in Chapter 3 of this book, and the basic diagram is shown in Figure 8.54. Note that in the normal string DAC configuration, the A and B terminals are connected between the reference voltage, and the W (wiper) terminal is the DAC output. There is also one more R resistor in the string DAC configuration which connects the A terminal to the reference.

The digital potentiometer configuration essentially makes use of the fact that the CMOS switches' common-mode voltages can be anywhere between the power supplies—the switch selected by the digital input simply connects the wiper to the corresponding tap on the resistor string. The relative polarity of A to B can be either positive or negative.

The resistor string represents the end-to-end potentiometer resistance, and the traditional "DAC output" becomes the wiper of the digital potentiometer. The resistors can be either polysilicon (TC ~ 500 ppm/°C) or thin film (TC ~ 35 ppm/°C), depending upon the desired accuracy.

The number of resistors in the string determines the resolution or "step size" of the potentiometer, and ranges from 32 (5 bits) to 1024 (10 bits) at present. The value of the programmable resistors are simply: $R_{WB}(D) = (D/2^N)\cdot R_{AB} + R_W$, and $R_{WA}(D) = [(2^N - D)/2^N]\cdot R_{AB} + R_W$, where R_{WB} is the resistance between W and B terminals, R_{WA} is the resistance between W and A terminals, D is the decimal equivalent of the step value, N is the number of bits, R_{AB} is the nominal resistance, and R_W is the wiper resistance.

The switches are CMOS transmission gates that minimize the on-resistance variations between any given step and the output. The voltages on the A and B terminals can be any value as long as they lie between the power supply voltages V_{DD} and V_{SS}.

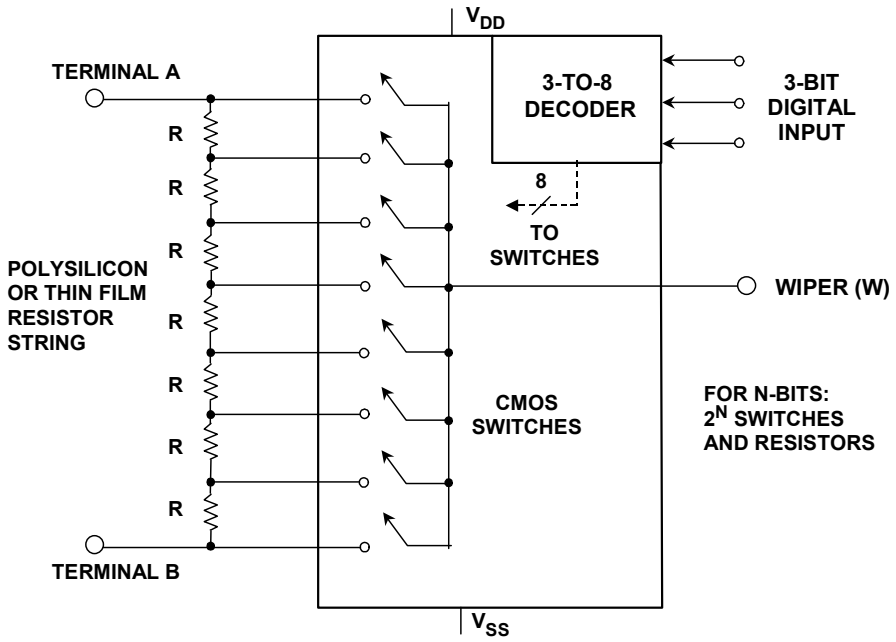


Figure 8.54: *3-Bit CMOS Digital Potentiometer Based on "String DAC" Architecture*

Modern Digital Potentiometers in Tiny Packages

Figure 8.55 shows three examples of digital potentiometers that are all offered in small packages. The I²C® serial interface is a very popular one, but digital potentiometers are also available with the SPI®, Up/Down Counter, and Manual Increment/Decrement interfaces.

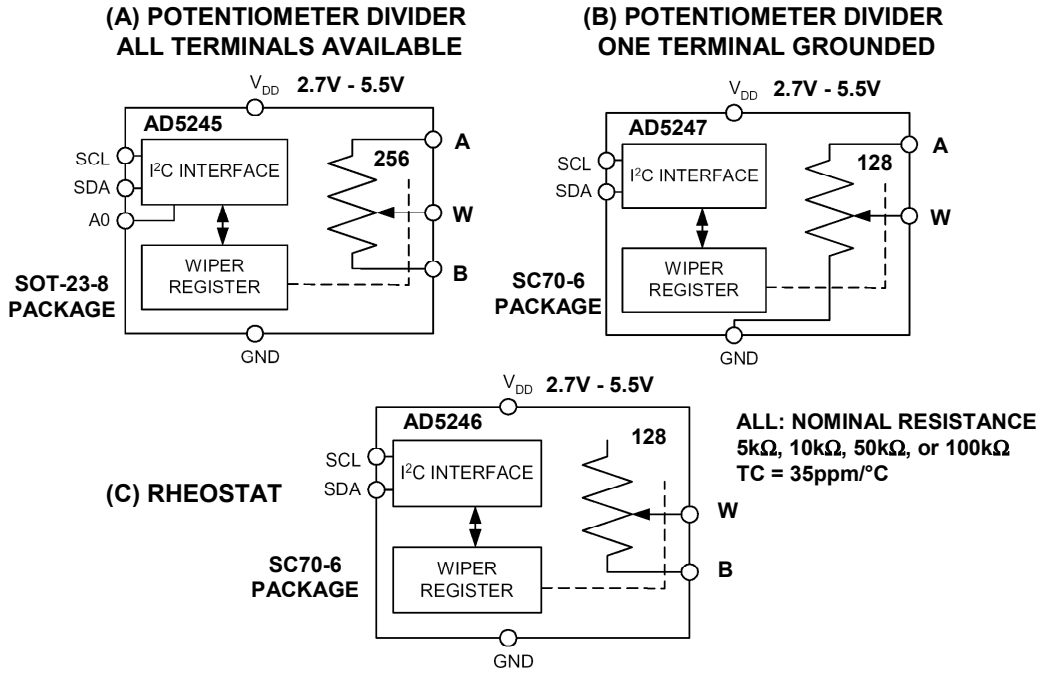


Figure 8.55: *Typical Examples of Digital Potentiometers in Tiny Packages*

The AD5245 shown in Figure 8.55A is available in an 8-lead SOT-23 package and has 256 positions (8-bits). The A0 pin allows the device to be uniquely identified so that two devices can be placed on the same bus. The thin film resistor string (R_{AB}) is available in 5 kΩ, 10 kΩ, 50 kΩ, or 100 kΩ, and the R_{AB} temperature coefficient is 35 ppm/°C. All three terminals of the potentiometer are available for use. The operating supply voltage can range from +2.7 V to +5.5 V. The power supply current is 8-µA maximum, and an internal command bit is available to shut down the device into a state of zero power consumption. The voltage noise is approximately the thermal noise of R_{AB}. (Recall that the thermal noise of a 1-kΩ resistor at room temperature is approximately 4 nV/√Hz).

The AD5247 shown in Figure 8.55B is similar to the AD5245, except it has 128 positions (7-bits), the B terminal is grounded, and the part comes in an SC70 6-lead package. The AD5247 does not have the A0 function. Finally, the AD5246 shown in Figure 8.55C is similar to the AD5245, but is connected as a rheostat with the W and B terminals available externally.

In addition to single potentiometers, such as the AD5245, AD5246, and AD5247, digital potentiometers are available as duals, triples, quads, and hex versions. Multiple devices per package offer 1% matching in ganged potentiometer applications as well as reducing PC board real estate requirements. Figure 8.56 summarizes some of the characteristics and features of modern digital potentiometers.

- **Resolution (wiper steps): 32 (5-Bits) to 1024 (10-Bits)**
- **Nominal End-to-End Resistance: 1kΩ to 1MΩ**
- **End-to-End Resistance Temperature Coefficient: 35ppm/°C (Thin Film Resistor String), 500ppm/°C (Polysilicon Resistor String)**
- **Number of Channels: 1, 2, 3, 4, 6**
- **Interface Data Control: SPI, I^2C, Up/Down Counter Input, Increment/Decrement Input**
- **Terminal Voltage Range: +15V, ±15V, +30V, +3V, ±3V, +5V, ±5V**
- **Memory Options:**
  - **Volatile (No Memory)**
  - **Nonvolatile E^2MEM**
  - **One-Time Programmable (OTP) - One Fuse Array**
  - **Two-Time Programmable - Two Fuse Arrays**

Figure 8.56: *Characteristics of CMOS Digital Potentiometers*

Digital Potentiometers with Nonvolatile Memory

Digital potentiometers, such as the AD5245, AD5246, and AD5247, are used mainly in active control applications, since they do not have non-volatile memory. Therefore, the setting is lost if power is removed. However, most volatile digital potentiometers have a power-on preset feature that forces the devices to the midscale code when power is applied.

Obviously, there is a demand for digital potentiometers with the ability to retain their setting after power is removed and reapplied. This requires the use of nonvolatile on-chip memory to store the desired setting. The AD5235 is an example of a dual 10-bit digital potentiometer which contains on-chip E^2MEM to store the desired settings (Reference 4). A functional block diagram is shown in Figure 8.57.

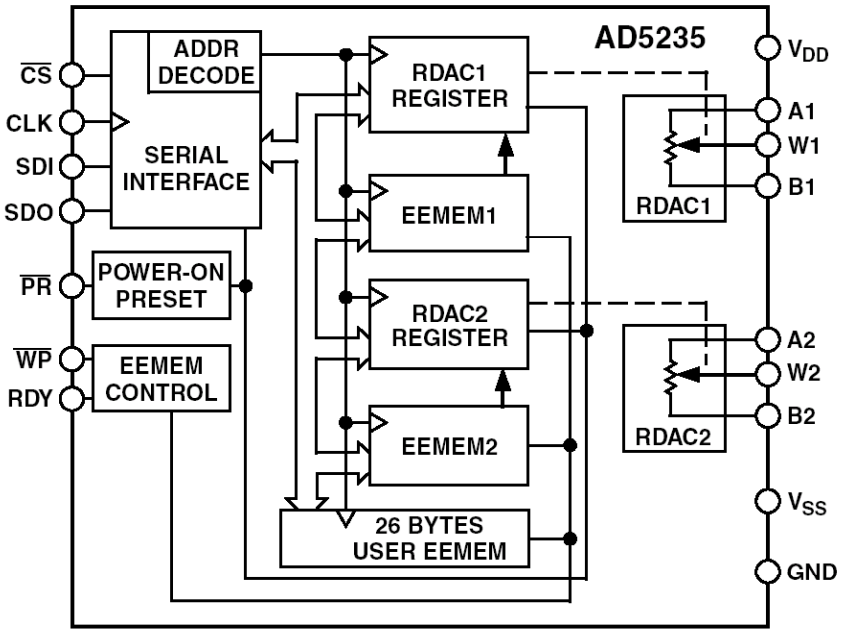


Figure 8.57: *AD5235 Nonvolatile Memory, Dual 1024-Position Digital Potentiometers*

These devices perform the same electronic adjustment function as a mechanical potentiometer with enhanced resolution, solid state reliability, and superior low temperature coefficient performance. The AD5235's versatile programming via a standard serial interface allows 16 modes of operation and adjustment, including scratch pad programming, memory storing and retrieving, increment/decrement, log taper adjustment, wiper setting readback, and extra user-defined E^2MEM. Another key feature of the AD5235 is that the actual resistance tolerance is stored in the E^2MEM at 0.1% accuracy. The actual end-to-end resistance can therefore be known, which is valuable for calibration and tolerance matching in precision applications. The new E^2MEM family of digital pots (AD5251/AD5252/AD5253/AD5254) also offer such a feature. In the scratch pad programming mode, a specific setting can be programmed directly to the RDAC register, which sets the resistance between terminals W-A and W-B. The RDAC register can also be loaded with a value previously stored in the E^2MEM register. The value in the E^2MEM can be changed or protected.

When changes are made to the RDAC register, the value of the new setting can be saved into the E^2MEM. Thereafter, it will be transferred automatically to the RDAC register during system power on. E^2MEM can also be retrieved through direct programming and external preset pin control. The linear step increment and decrement commands cause the setting in the RDAC register to be moved UP or DOWN, one step at a time. For logarithmic changes in wiper setting, a left/right bit shift command adjusts the level in

±6-dB steps. The AD5235 is available in a thin TSSOP-16 package. All parts are guaranteed to operate over the extended industrial temperature range of –40°C to +85°C.

One-Time-Programmable (OTP) Digital Potentiometers

The AD5172/AD5173 are dual channel 256-position, one-time programmable (OTP) digital potentiometers, which employ fuse link technology to achieve the memory retention of resistance setting function (Reference 5). A functional block diagram is shown in Figure 8.58. Note that the AD5172 is configured as a three-terminal potentiometer, while the AD5173 is pinned out as a rheostat. The AD5172/AD5173 is available in 2.5-kΩ, 10-kΩ, 50-kΩ, and 100-kΩ versions. The temperature coefficient of the resistor string is 35 ppm/°C. The power supply voltage can range from 2.7 V to 5.5 V.

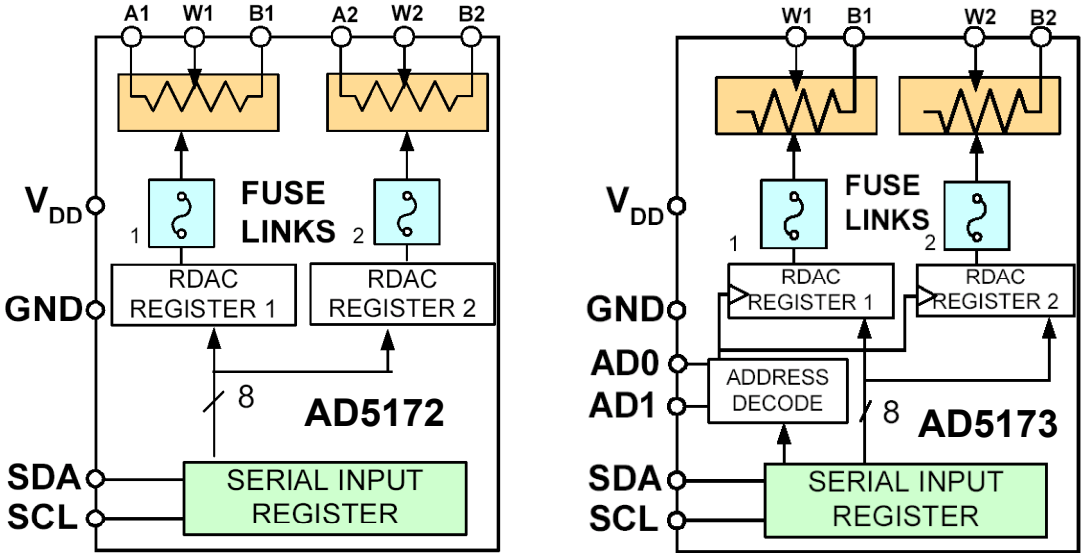


Figure 8.58: *AD5172/AD5173 256-Position One-Time Programmable Dual-Channel I²C Digital Potentiometer*

OTP is a cost-effective alternative over the E²MEM approach for users who do not need to program the digital potentiometer setting in memory more than once, i.e., "set and forget." These devices perform the same electronic adjustment functions most mechanical trimmers and variable resistors do but offer enhanced resolution, solid-state reliability, and better temperature coefficient performance.

The AD5172/AD5173 are programmed using a 2-wire I²C compatible digital control. They allow unlimited adjustments before permanently setting the resistance value. During the OTP activation, a permanent fuse blown command is sent after the final value is determined; therefore freezing the wiper position at a given setting (analogous to placing epoxy on a mechanical trimmer). Unlike other OTP digital potentiometers in the same family, AD5172/AD5173 have a unique temporary OTP overwriting feature that allows new adjustments if desired, the OTP setting is restored during subsequent power up conditions. This feature allows users to apply the AD5172/AD5173 in active control applications with user-defined presets.

To verify the success of permanent programming, Analog Devices patterned the OTP validation such that the fuse status can be discerned from two validation bits in read mode. For applications that program AD5172/AD5173 in the factories, Analog Devices offers device programming software, which operates across Windows® 95 to XP® platforms including Windows NT®. This software application effectively replaces the need for external I²C controllers or host processors and therefore significantly reduces users' development time. An AD5172/AD5173 evaluation kit is available, which include the software, connector, and cable that can be converted for factory programming applications. The AD5172/AD5173 are available in a MSOP-10 package. All parts are guaranteed to operate over the automotive temperature range of −40°C to +125°C. Besides their unique OTP features, the AD5172/AD5173 lend themselves well to other general-purpose digital potentiometer applications due to their programmable preset, superior temperature stability, and small form factor.

The AD5170 (Reference 6) is a two-time programmable 8-bit digital potentiometer, and a functional diagram is shown in Figure 8.59. Note that a second fuse array is provided to allow "second chance" programmability. Like the AD5172/AD5173, there is unlimited programmability before making the permanent setting. The electrical characteristics of the AD5170 are similar to the AD5172/AD5173.

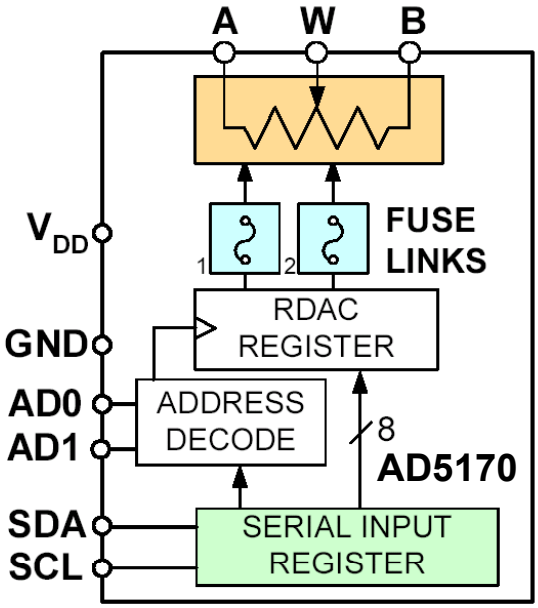


Figure 8.59: *AD5170 256-Position Two-Time Programmable I²C Digital Potentiometer*

Digital Potentiometer AC Considerations

Digital potentiometers can be used in ac applications, provided the bandwidth limitations created by the internal capacitance are considered. Figure 8.60 shows an ac model of a digital potentiometer, where the capacitances are modeled as C_A, C_B, and C_W. The bandwidth of the digital pot is configuration dependent. It is also dynamic because of the variable resistance. For example, if A terminal is the input, B terminal is grounded, and W terminal is the output; then the bandwidth can be approximated by BW = $1/[2\pi(R_{WB}||R_{WA})\cdot C_W]$. The lowest bandwidth occurs at midscale, where the equivalent resistance is at its maximum in this configuration. The typical values for the AD5245 are shown as well as the corresponding bandwidths for the various resistance options measured at midscale. This simple model can be used in SPICE simulations to predict circuit performance, such as when the digital potentiometer is used as a part of the feedback network of an op amp. The other issue to consider when placing digital potentiometers directly in the signal path is their slightly nonlinear resistance as a function of applied voltage. This effect leads to a small amount of distortion. For example, the AD5245 has a THD of 0.05% when a 1-V rms, 1-kHz signal is applied to the configuration described above at midscale. References 10, 11, 14, 15, and 17 show excellent examples of the application of digital potentiometers in ac applications.

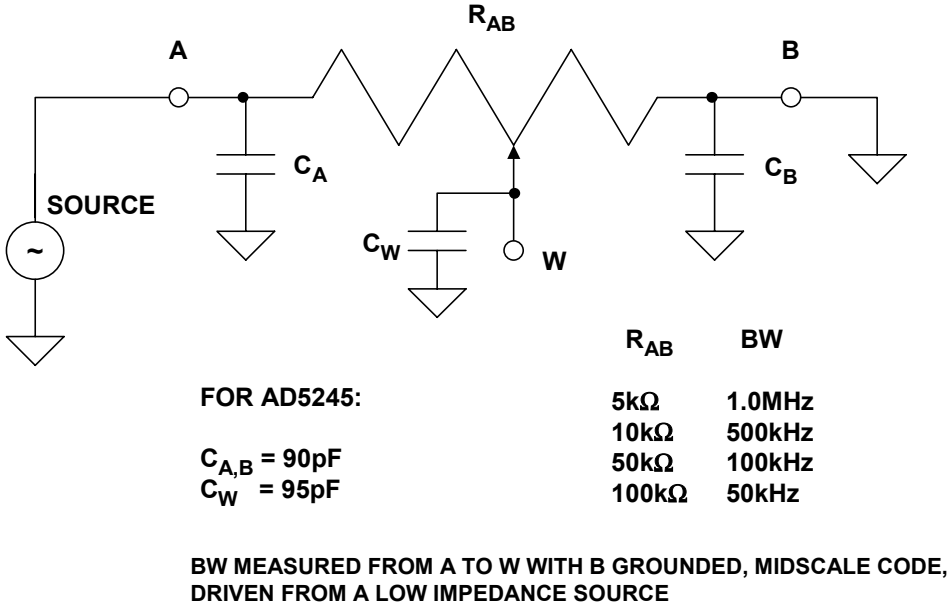


Figure 8.60: *Digital Potentiometer Bandwidth Model*

Application Examples

Like op amps, digital pots are the building blocks of many electronic circuits. Because they are digitally controlled, digital pots can be used in active control applications, in addition to basic trimming or calibration applications. For example, digital pots can be used in programmable power supplies as shown in Figure 8.61A. Typical adjustable low dropout voltage regulators (such as the anyCAP series) have a FB pin, where applying a resistor divider yields a variable output voltage. As shown, R1 and R2 are the feedback

and input resistors, respectively. The FB circuit has an internal non-inverting amplifier which gains up a 1.2-V bandgap reference to the desired output voltage.

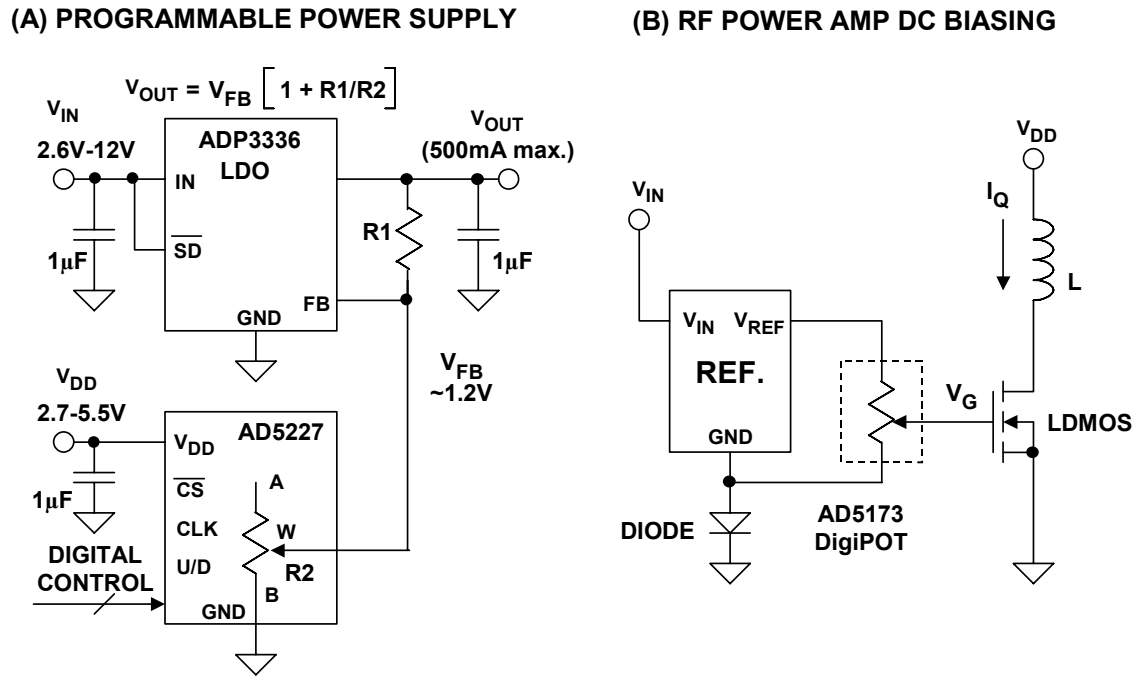


Figure 8.61: *Two Circuit Applications for Digital Pots*

Similarly, electronic equipment makers use digital potentiometers in power supplies by adjusting the supplies to the tolerances that cover all supply voltage conditions during reliability testing. This voltage-margining approach accelerates the burn-in process, and therefore reduces the system time-to-market.

Because of the optimized cost/performance benefits, digital pots have been gaining popularity in replacing traditional DACs in many applications. For example, in wireless basestations, the optimum threshold voltages of the RF power amplifiers vary widely in production. Such variation affects the transmitted signal linearity and power efficiency. Too much power delivered from a poorly regulated amplifier can also interfere with neighboring cells within the wireless network. Although DACs are widely used in biasing RF power amplifiers, many users find digital pots to be more suitable in such applications because of the availability of non-volatile memory, which simplifies the designs. As shown in Figure 8.61B, the one-time-programmable digital pot is used to calibrate the dc bias point of the RF power amplifier, and the calibration is programmed by factory software without the need for any external controllers. Note that the diode is added to the circuit to compensate for the amplifier's temperature coefficient.

Summary

Digital potentiometers offer many obvious advantages over mechanical potentiometers and trimpots®, and therefore they have become widely accepted in modern systems. Their reliability, flexibility, and ease of use makes them popular replacements for the traditional potentiometer. Digital pots can also be used as programmable building blocks in many active control applications.

There are virtually endless applications for digital potentiometers in modern electronic systems—one only has to consider the many traditional applications for mechanical pots and trimpots as a starting point. References 7-18 should be consulted for more ideas on how these devices can enhance a design. A few applications are summarized below:

- *General Purpose Applications:* sensor calibration, system gain and offset adjustments, programmable gain amplifiers, programmable filters, programmable set-points, traditional digital-to-analog converters, voltage-to-current converters, line impedance matching.

- *Computer and Network Equipment:* programmable power supplies, power supply margining, battery charger set-points, temperature control set-points.

- *LCD Displays:* backlight, contrast, and brightness adjustments, LCD panel common voltage adjustment, programmable gamma correction, LCD projector reference voltage generator.

- *Consumer Applications:* PDA backlight adjustment, electronic volume controls.

- *RF Communications:* RF power amplifier biasing, DDS/PLL amplitude adjustment, VCXO frequency tuning, varactor diode biasing, log amp slope and intercept adjustment, quadrature demodulator gain and phase adjustment, RFID reader calibration.

- *Automotive:* set-points in the engine control unit, sensor calibrations, actuator controls, instrumentation control, navigation/entertainment display adjustments.

- *Industrial and Instrumentation:* system calibration, floating reference DACs, programmable 4-to-20-mA current transmitters.

- *Optical Communications:* laser bias current adjustments, laser modulation current adjustments, optical receiver signal conditioning, optical attenuators, wavelength controllers.

REFERENCES:
8.3 DIGITAL POTENTIOMETERS

1. Data sheet for AD5245 256-Position I^2C Compatible Digital Potentiometer, http://www.analog.com.

2. Data sheet for AD5247 128-Position I^2C CompatibleDigital Potentiometer, http://www.analog.com.

3. Data sheet for AD5246 128-Position I^2C CompatibleDigital Resistor, http://www.analog.com.

4. Data sheet for AD5235 Nonvolatile Memory, Dual 1024-Position Digital Potentiometers, http://www.analog.com.

5. Data sheet for AD5172 256-Position One-Time Programmable Dual-Channel I^2C Digital Potentiometer, http://www.analog.com.

6. Data sheet for AD5170 256-Position Two-Time Programmable I^2C Digital Potentiometer, http://www.analog.com.

7. Walt Heinzer, "Design Circuits with Digitally Controllable Variable Resistors," Analog Dialogue, Vol 29, No. 1, 1995, http://www.analog.com.

8. Hank Zumbahlen, "Tack a Log Taper onto a Digital Potentiometer," **EDN**, January 20, 2000.

9. Mary McCarthy, "Digital Potentiometers Vary Amplitude In DDS Devices," **Electronic Design**, Ideas for Design, May 29, 2000.

10. Alan Li, "Versatile Programmable Amplifiers Use Digital Potentiometers with Nonvolatile Memory," **Analog Dialogue**, Vol. 35, No. 3, June-July, 2001.

11. Reza Moghimi, "Difference Amplifier Uses Digital Potentiometers ," **EDN**, May 30, 2002.

12. Mark Malaeb, "Single-Chip Digitally Controlled Data-Acquisition as Core of Reliable DWDM Communication Systems," **Analog Dialogue**, Vol. 36, No. 5, September-October, 2002, http://www.analog.com.

13. Peter Khairolomour, "Rotary Encoder Mates with Digital Potentiometer," **EDN**, Design Idea, March 6, 2003.

14. Alan Li, "Versatile Programmable Amplifiers Using Digital Potentiometers with Nonvolatile Memory," **Application Note AN-579**, http://www.analog.com.

15. Alan Li, "Programmable Oscillator Uses Digital Potentiometers," **Application Note AN-580**, http://www.analog.com.

16. Alan Li, "Resolution Enhancements of Digital Potentiometers with Multiple Devices," **Application Note AN-582**, http://www.analog.com.

17. Alan Li, "AD5232 Programmable Oscillator Using Digital Potentiometers, " **Application Note AN-585**, http://www.analog.com.

18. Alan Li, " ADN2850 Evaluation Kit User Manual," **Application Note AN-628**, Analog Devices, http://www.analog.com.

SECTION 8.4: DIGITAL AUDIO

Walt Kester

Introduction

Voiceband digital audio had its beginnings back in the early days of the PCM system development initiated by the 1937 patent filing of A. H. Reeves of the International Telephone and Telegraph Corporation (Reference 1). During the early 1940s, Bell Telephone Laboratories continued PCM work relating to speech encryption systems, and after the war, turned their attention to commercial PCM transmission. An experimental 24-channel PCM system was developed, and the results summarized in 1948 in Reference 2 by L. A. Meacham and E. Peterson. Some of the significant developments of this work were the successive approximation ADC, Shannon-Rack decoder (DAC), and the logarithmic companding/expanding of voiceband signals.

In order to minimize the number of bits per second and still maintain the required dynamic range for voiceband, the early system utilized 7-bit ADCs and DACs with a logarithmic compressor ahead of the ADC and a logarithmic expander after the DAC.

With the solid state devices available in the mid 1950s, Bell Labs developed the T-1 carrier system which was prototyped in the late 1950s and put into service in the 1960s. The standard sampling rate for voiceband signals was established at 8 kSPS, and the initial system used 7-bit logarithmically encoded ADCs and DACs. Later systems used 8-bit "segmented" ADCs and DACs (see Chapter 3 of this book for a description of the architecture).

Modern wireless systems, such as cellular telephone, use higher resolution *linear* Σ-Δ ADCs and DACs, rather than the *logarithmic* ones used in the early systems. A simplified comparison between the standard 8-bit companded system and the modern cell phone handset is shown in Figure 8.62. Modern cellular transmission systems make use of sophisticated DSP-based speech compression algorithms in order to reduce the overall data rate to acceptable levels, rather than limiting the resolution of the converters. In most cases the ADC and DAC (codec) are integrated into a chip which performs many other digital functions in a handset. It should be noted that if needed, the modern linear codecs can be made backward compatible with the logarithmically encoded 8-bit systems by simply using on-chip lookup tables to convert the high resolution linear data into the 8-bit logarithmic data.

In the 1970s and 1980s, the field of digital audio rapidly expanded to include much more than voiceband for PCM systems. A driving force behind this expansion was the increased availability of low-cost high resolution ADCs and DACs with sufficient dynamic range and sampling rates.

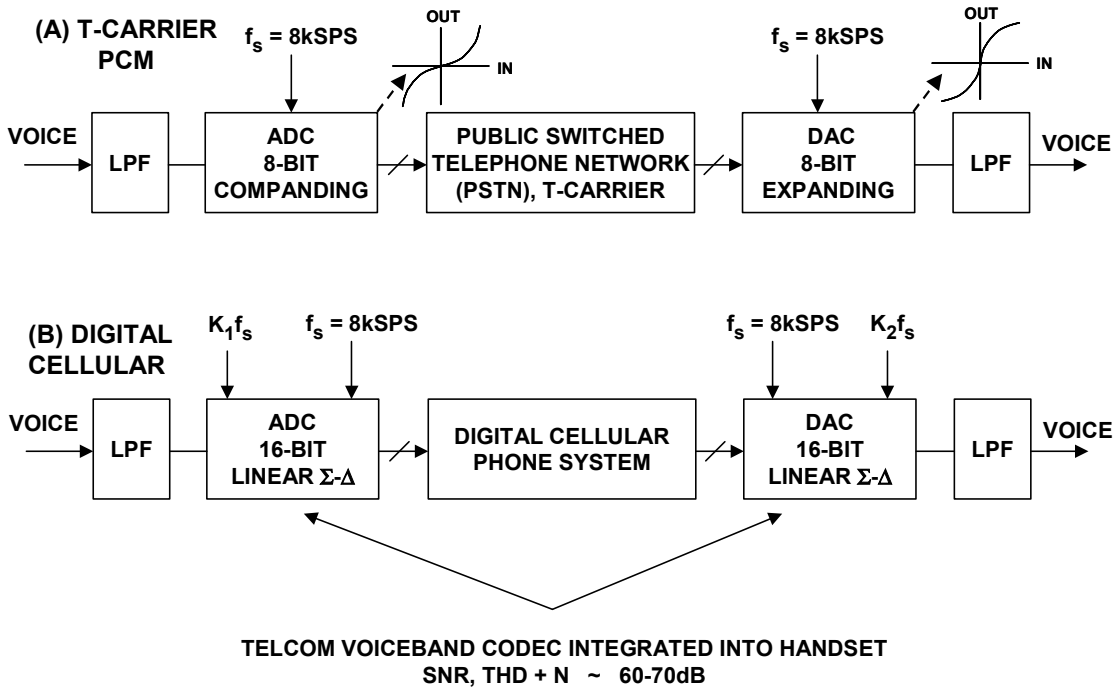


Figure 8.62: *Voiceband Telcom Digital Audio Simplified*

In the consumer electronics industry, the compact disk (CD) player has proliferated into nearly every household. Today, high-end DVD audio players give increased levels of performance in home theater systems.

Since the beginning of the 1980s, digital audio equipment has steadily been replacing analog equipment in broadcast and production systems. Some of this digital equipment has analog inputs and outputs and is designed to replace an analog device and operate in an analog environment (i.e., a digital "black box"). However, the trend in broadcast and production is toward the all-digital studio, in which all aspects of recording, processing, and transmission take place in the digital domain. To this end, the AES (Audio Engineering Society) and EBU (European Broadcast Union) have developed standards to facilitate this future transition.

Sampling Rate and THD + N Requirements for Digital Audio

The key audio specifications are total harmonic distortion plus noise (THD + N), dynamic range (DNR), and signal-to-noise ratio (SNR). THD + N is more correctly expressed as (THD + N)/S the ratio of the rms sum of all spectral components in the passband (20 Hz to 20 kHz), excluding the fundamental, to the rms value of the fundamental input signal. The ratio can be expressed in % or dB. THD + N is a negative number when expressed in dB, but often simply expressed as a positive number, with the minus sign assumed.

Dynamic range (DNR) is the ratio of a fullscale input signal to the integrated noise in the passband (20 Hz to 20 kHz), expressed in dB. It is measured with a –60-dB input signal

and is equal to [S/(THD+N)] + 60dB. The noise level therefore basically establishes the dynamic range. It is specified with and without an A-Weight filter applied.

Signal-to-noise ratio (SNR) is the ratio of the fullscale input signal level to the integrated noise in the passband (20 Hz to 20 kHz) with no input signal applied, expressed in dB (a positive number). In many cases, the SNR and DNR specifications are approximately equal. Note that this definition of SNR for audio is slightly different than the SNR for standard ADCs and DACs defined in Chapter 2, where it is defined as the ratio of the rms signal to rms value of all other components excluding the harmonics of the fundamental. These definitions are summarized in Figure 8.63.

- **Total Harmonic Distortion Plus Noise (THD + N):**
  - **More correctly: S/(THD + N), the ratio of the rms value of the fundamental input signal to the rms sum of all other spectral components in the passband (20Hz to 20kHz), expressed in % or dB. This is a negative number in dB, but often simply expressed as a positive number, with the minus sign assumed.**
- **Dynamic Range (DNR):**
  - **The ratio of a fullscale input signal to the integrated noise in the passband (20Hz to 20kHz), expressed in dB. It is measured with a –60dB input signal and is equal to [S/(THD+N)] + 60dB, so the noise level establishes the dynamic range. It is specified with and without an A-Weight filter applied.**
- **Signal-to-Noise Ratio (SNR):**
  - **The ratio of the fullscale input signal level to the integrated noise in the passband (20Hz to 20kHz) with no input signal applied, expressed in dB. (Approximately equal to DNR in many cases)**

Figure 8.63: *Key Audio Specifications*

Figure 8.64 lists a few of the popular applications of digital audio and some typical THD + N and sample rate requirements. For the purposes of this discussion, THD + N numbers are given as positive numbers in dB below the signal level. In actuality, when a small percentage, for example 0.001% is converted into dB, it is a negative number as previously mentioned above.

In most cases, the sampling frequency is chosen to be slightly above twice the highest frequency of interest, however, the actual numbers deserve some further discussion.

The early requirement for the standard PCM T-carrier sampling rate of 8 kSPS has already been discussed. Voiceband audio occupies an approximate bandwidth of 3.5 kHz, and requires an SNR of only 60 dB to 70 dB. Although 16-bit Σ-Δ codecs are used today for the convenience of DSPs, only approximately 11-bits of actual dynamic range is required.

FM stereo has a higher bandwidth (typically 15 kHz), and a sampling rate of 32 kSPS was therefore chosen for digital transmission over land lines connecting the studio to FM transmitter. A minimum THD + N of 60 dB to 70 dB is sufficient for these applications.

	THD + N (dB)	Standard Sample Rates (kSPS)
Telcom	60 - 70	8
FM Stereo	60 - 70	32
Speech Analysis, etc.	70 - 80	8 - 48
Computer Audio	80 - 90	48
Stereo CD, DAT, etc.	> 100	44.1, 48, 88.2, 96
DVD Audio	> 100	48, 96, 192

Figure 8.64: *Digital Audio THD + N and Sample Rate Requirements*

Speech analysis and speech processing systems require a THD + N of at least 70 dB to 80 dB, and sampling rates up to 48 kSPS are used, depending upon the application.

The professional audio bandwidth extends from 20 Hz to 20 kHz. Therefore, a minimum sampling frequency of 40 kSPS is required—in practice, 44.1 kSPS (audio CD standard) is the lowest used.

High quality computer audio sound cards need 80 dB to 90 dB THD + N, and 48 kSPS has been adopted as the standard sampling frequency.

High-end stereo CD players, DVD audio players, and studio recording systems require greater than 100 dB of THD + N and DNR, and therefore place the most critical requirements on the ADC and DAC. Regarding sampling frequency, 44.1 kSPS was chosen as the compact standard sampling frequency. It was selected to allow the use of NTSC or PAL "U-Matic" videotape recorders (VTRs) fitted with a PCM adapter to record and play back digital audio signals transformed into "pseudo-video" waveforms. Later, these VTRs were used to master compact disks (CDs), and 44.1 kSPS became a defacto standard that is also used in some digital audio tape (DAT) play-back-only applications.

For studio and broadcast applications, 48-kSPS sampling has become the industry standard for digital audio recording. This frequency was adopted for the following reason. In a digital television environment, the digital audio reference signal must be locked to the video reference signal to avoid drift in the relationship between audio and video signals and allow click-free audio and video switching. A sampling rate of 48 kSPS was chosen for both NTSC and PAL to facilitate the conversion between the two standards and maintain the proper phase relationship between video and audio in both systems (the details of this are explained in Reference 1). In these applications, THD + N requirements are generally greater than 100 dB.

Audio for digital video disk (DVD) utilizes sampling frequencies of 48 kSPS when video and audio are both present. Although most humans cannot hear frequencies above 20 kHz, tests have shown that harmonics and the effects of room acoustics enable some audio above 20 kHz to be heard, or at least felt. Therefore, for high-end DVD audio-only applications, sampling rates of 96 kSPS and 192 kSPS can be used. Higher DVD sampling frequencies and resolution enhance the audio quality over CDs in stereo playback (i.e., 96-kSPS/24-bit vs. 44.1 kSPS/16-bit for CDs). THD + N and DNR requirements for DVD audio are typically greater than 100 dB.

Pulse Code Modulation (PCM) is the basic form of digital audio used on most CDs as well as to master virtually all digital recording. PCM encoding on DVD-video products can use up to a 96-kSPS sampling frequency and a 24-bit sample word. Producers of DVD products rely heavily on audio and video compression to fit their source material within the space and bandwidth of the DVD medium. By slightly compressing the audio, DVD producers can make space available for video and other added features without sacrificing perceptible audio performance and quality. The audio compression formats are used only to remove redundant data. The end user does not detect the difference, because the removed data is masked by other sounds. Since the incoming audio stream is altered by the compression, all of the original PCM data cannot be recovered on playback—these formats are referred to as lossy compression. This can result in audio tracks as small as 1/15th the size of the uncompressed PCM master for Dolby Digital compression.

Overall Trends in Digital Audio ADCs and DACs

Digital audio systems place high performance demands on ADCs and DACs because of the wide dynamic range requirements. Early ADCs for digital audio in the 1970s typically utilized either the successive approximation or subranging architectures (see Chapter 3 for architecture descriptions). The resolution was generally 16-bits, and the maximum sampling frequency about 50 kSPS. The ADCs were modules or hybrids, and the DACs were ICs with an input serial-to-parallel converter followed by a traditional parallel binarily-weighted DAC. The DACs generally used thin-film laser trimmed resistors to achieve the required accuracy. The ADCs were relatively costly and primarily used in the recording studios, while the DACs were used in high volume in consumer CD players.

Early CD players used techniques similar to the simplified diagram in Figure 8.65A. The output anti-imaging filter presents a fundamental problem with this approach, especially when audio requirements are considered. Theoretically, a 16-bit parallel DAC updated at 44.1 kSPS could be used at the output, however, because the audio bandwidth extends to 20 kHz, the transition region of the filter is narrow. For example, with a 44.1 kSPS update rate, the transition region is from 20 kHz to 24 kHz, which is $\log_2(24 \div 20) = \log_2(1.2) = 0.263$ octaves. For 60-dB stopband attenuation in 0.263 octaves, the required slope of the filter in the transition region is $60 \div 0.263 = 228$ dB/octave. Assuming 6-dB/octave per pole, a 38-pole filter would be required! This is obviously a difficult and expensive filter, especially if linear phase is desired (as is the case in audio applications). Another problem is the "sin(x)/x" rolloff caused by the DAC reconstruction process.

With no compensation, the output is attenuated by approximately 4 dB at the Nyquist frequency of 22.05 MHz (see Chapter 2 of this book for details).

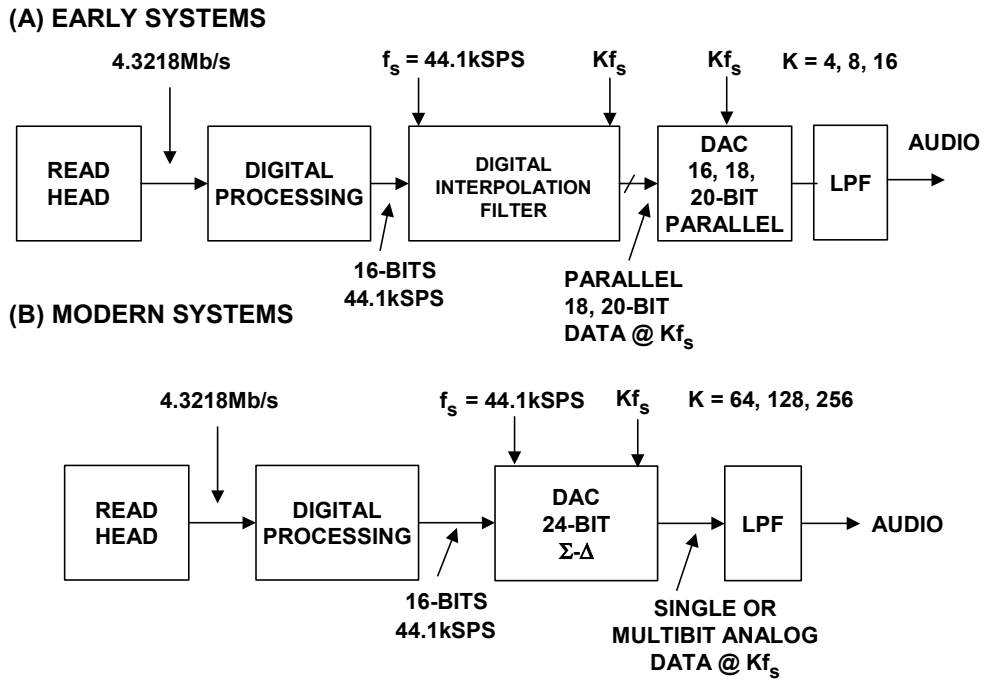


Figure 8.65: *Stereo CD Digital Audio Simplified (One Channel Shown)*

Therefore, in order to simplify the anti-imaging filter requirement, oversampling techniques are used as shown. The 16-bit, 44.1-kSPS data is passed through a digital interpolation filter which creates extra data points, and produces output data at a multiple K times the original sampling rate of 44.1 kSPS. A side benefit from oversampling is the 3-dB increase in SNR that occurs each time the output sample rate is doubled. Oversampling rates of 4, 8, and 16 were popular in early CD players. With K = 16, for example, the effective output update rate is now $16 \times 44.1 = 705.6$ kSPS. The transition region of the filter now extends from 20 kHz to 685.6 kHz, which is equal to $\log_2(685.6 \div 20) = \log_2(34.3) = 5.1$ octaves. The required slope of the filter in the transition region is now $60 \div 5.1 = 12$ dB/octave, and a 2 or 3-pole filter is sufficient. The high oversampling rate also minimizes the signal attenuation due to the sin(x)/x rolloff previously mentioned.

The Σ-Δ ADC uses a highly oversampled input analog modulator followed by a digital filter and decimator, as described in detail in Chapter 3 of this book. The Σ-Δ DAC uses a digital modulator to produce a single (or multibit) analog output at a highly oversampled rate. The oversampling feature greatly eases the requirements on both the ADC input antialiasing filter and the DAC output anti-imaging filter. There are many other advantages of the Σ-Δ architecture which make it the ideal choice for audio ADCs and DACs. Figure 8.65B shows a modern CD player using a Σ-Δ DAC, where oversampling rates of 64, 128, and 256 are quite commonly used.

Today, Σ-Δ ADCs and DACs dominate the digital audio market because of their high dynamic range, oversampling architecture, low power, and relatively low cost. Because

they are typically produced on CMOS processes, the addition of many audio-specific digital features is relatively easy. The following sections examine a few of the many digital audio offerings available from Analog Devices.

Voiceband Codecs

There are many applications where both an ADC and a compatible DAC are required, such as in voice and audio processors, digital video camcorders, cell phone handsets, PC sound cards, etc. When the ADC and DAC are both on the same chip, they are called a *coder-decoder* (or codec). The AD74122 (Reference 4) is a typical example of a low cost, low power general purpose stereo voice and audio bandwidth codec. A simplified block diagram is shown in Figure 8.66.

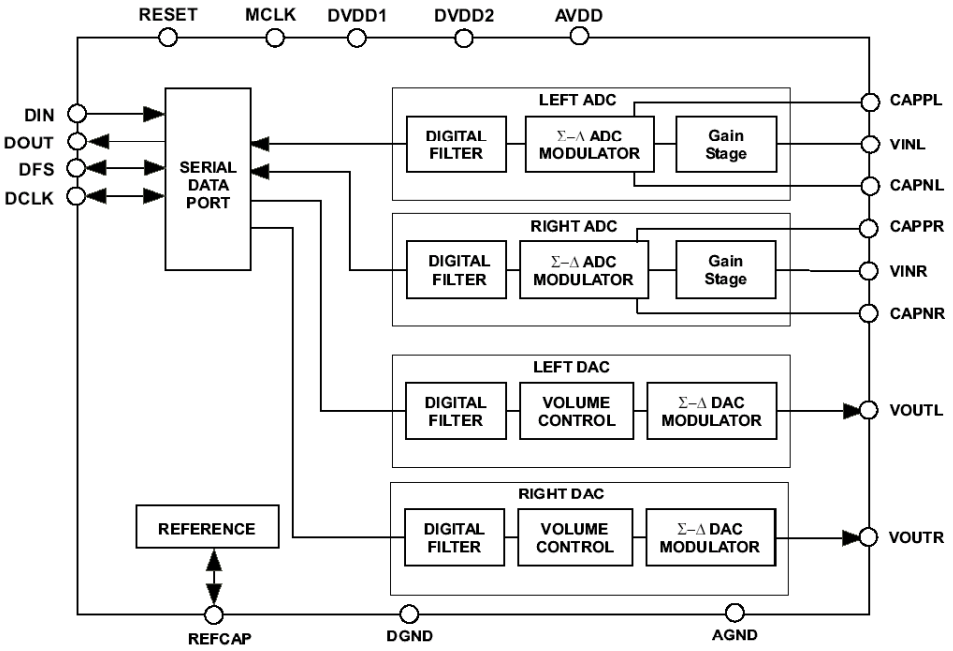


Figure 8.66: *AD74122 16-/20-/24-Bit, 48-kSPS Stereo Voiceband Codec*

The AD74122 is a 2.5-V Σ-Δ stereo audio codec with 3.3-V tolerant digital interface. It supports sampling rates from 8 kSPS to 48 kSPS and provides 16-/20-/24-bit word lengths. The architecture uses multibit modulators and data directed scrambling DACs for reduced idle tones and noise floor (see Chapter 3 of this book).

The ADC THD + N in the 20 Hz to 20 kHz bandwidth is 67 dB and the dynamic range (DNR) is 85 dB. The DAC THD + N is 88 dB (measured with a sampling rate of 48 kSPS), and the dynamic range is 93 dB. The device has digitally programmable input/output gain, on-chip volume controls per output channel, software controllable clickless mute, and contains an on-chip reference. The serial interface is compatible with popular DSPs. The AD74122 is packaged in a 20-lead TSSOP package.

High Performance Audio ADCs and DACs in Separate Packages

For studio quality digital audio recording, the THD + N and SNR of an ADC should be greater than 100 dB. Early ADCs for digital audio were expensive modules or hybrids, now of course, they are ICs based on the Σ-Δ architecture. The AD1871 stereo 24-bit, 96-kSPS Σ-Δ ADC is an excellent example of an ADC suitable for the exacting requirements of professional audio recording (Reference 5). It uses multibit modulators and data scrambling techniques to yield 103-dB THD + N, and 105-dB SNR/DNR. The device operates at an input oversampling frequency of 6.144 MSPS for an output sampling rate of 48 kSPS (K = 128). It has an SPI-compatible serial port, on-chip reference, and is housed in a 28-lead SSOP package. A functional diagram is shown in Figure 8.67.

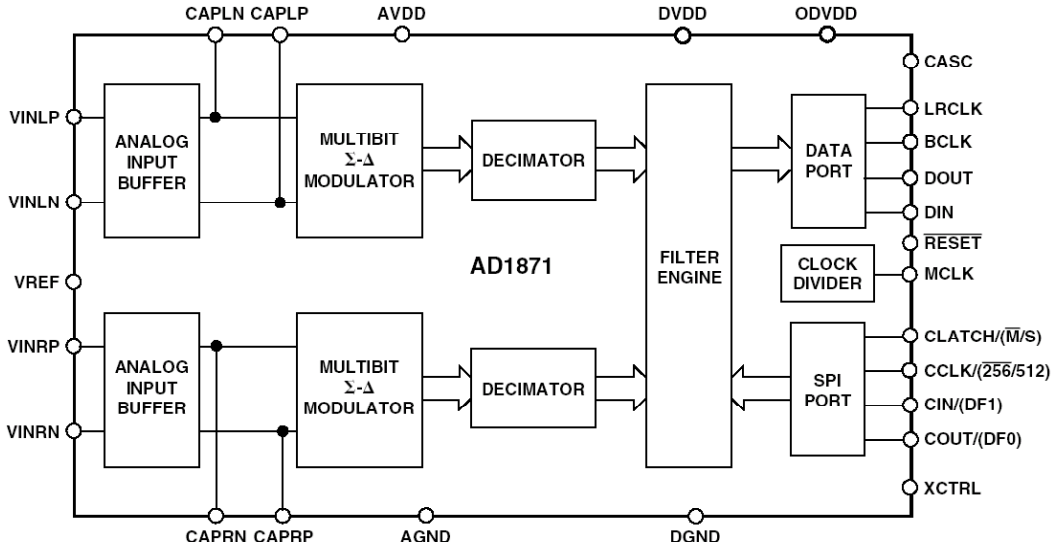


Figure 8.67: *AD1871 Stereo Audio, 24-Bit, 96-kSPS Multibit Σ-Δ ADC*

Looking at DACs, the AD1955 (Reference 6) represents the high-end of digital audio performance. It operates on a 5-V power supply and 16-/18-/20-/24-bit data at up to a 192-kSPS sample rate. It supports the SACD (super audio compact disk, a Phillips standard) DSD (direct stream digital) bit stream, and supports a wide range of PCM sample rates including 32 kSPS, 44.1 kSPS, 48 kSPS, 88.2 kSPS, 96 kSPS, and 192 kSPS. The AD1955 uses a multibit Σ-Δ modulator with "Perfect Differential Linearity Restoration" and data directed scrambling for reduced idle tones and noise floor. The output is a differential current of 8.64-mA p-p.

The AD1955 has 120-dB SNR/DNR at a 48-kSPS sample rate (A-Weighted stereo) and 110-dB THD + N. The digital filter has 110-dB stopband attenuation with ±0.0002-dB passband ripple. The device has hardware and software controllable clickless mute, serial (SPI) interface, and is housed in a 28-lead SSOP plastic package. A functional diagram is shown in Figure 8.68.

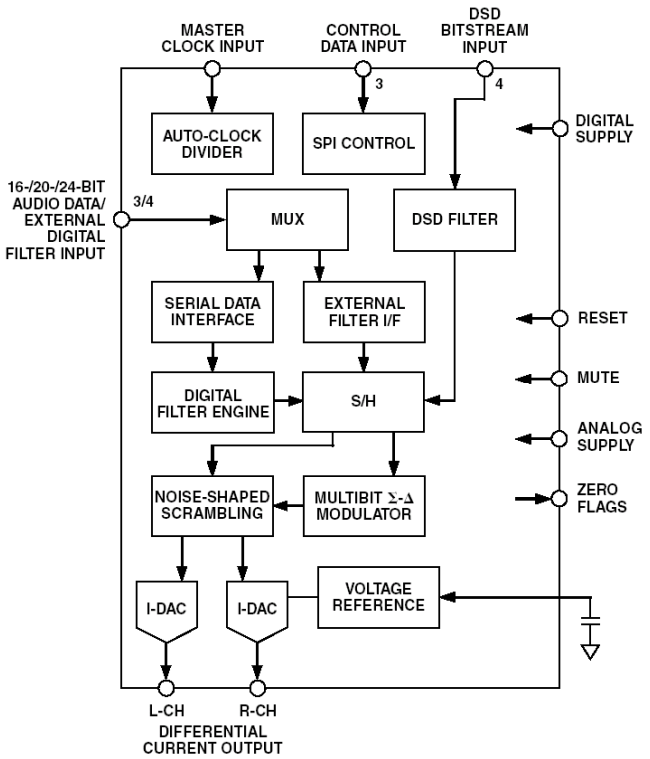


Figure 8.68: *AD1955 High Performance Multibit Σ-Δ DAC*

Figure 8.69 summarizes the current (2004) Analog Devices portfolio of high-end stereo audio DACs in individual packages.

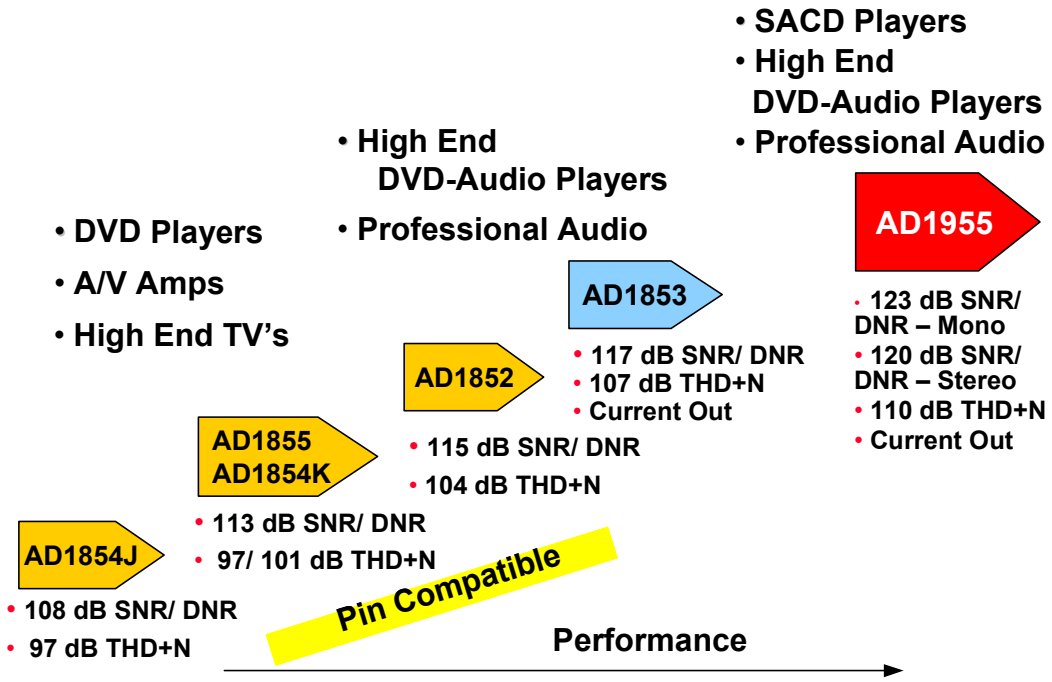


Figure 8.69: *Audio DAC Family*

The CMOS processes used to fabricate Σ-Δ ADCs and DACs lend themselves to additional digital functionality with only moderate increases in chip real estate and power. The SigmaDSP™ family of audio DACs incorporate DSPs which allow speaker equalization, dual-band compression/limiting, delay compensation, and image enhancement. These algorithms can be used to compensate for real-world limitations of speakers, amplifiers, and listening environments, resulting in a dramatic improvement in perceived audio quality.

The AD1953 SigmaDSP 3-channel, 26-bit signal processing DAC (Reference 7) accepts data at sample rates up to 48 kSPS. The signal processing used in the AD1953 is comparable to that found in high-end studio equipment. Most of the processing is done in full 48-bit double-precision mode, resulting in very good low level signal performance and the absence of limit cycles or idle tones. The compressor/limiter uses a sophisticated two-band algorithm often found in high-end broadcast compressors. A simplified block diagram is shown in Figure 8.70.

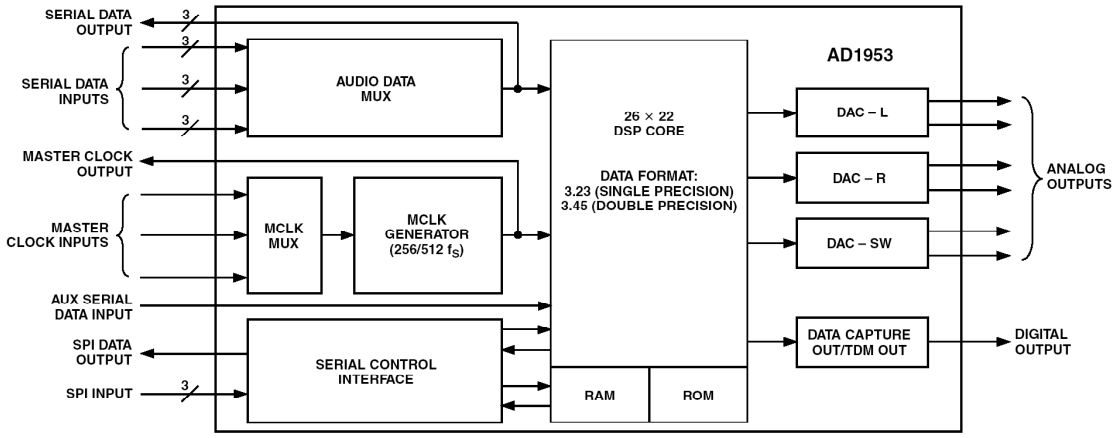


Figure 8.70: *AD1953 SigmaDSP™ 3-Channel, 26-Bit Signal Processing DAC*

The AD1953 has a dynamic range of 112 dB and a THD + N of 100 dB. Note that the DAC has left and right channels as well as a subwoofer output channel. The part operates from a single 5-V supply and is housed in a 48-lead LQFP package. A graphical user interface (GUI) is available for evaluation of the AD1953 as shown in Figure 8.71. This GUI controls all of the functions of the chip in a very straightforward and user-friendly interface. No code needs to be written to use the GUI to control the device. Software development tools are also available.

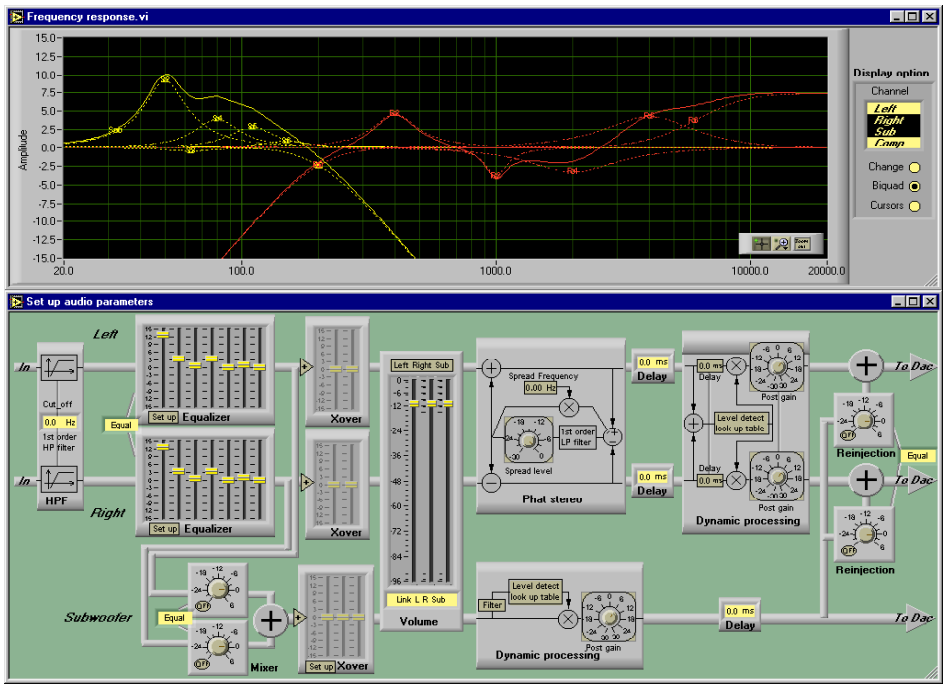


Figure 8.71: *AD1953 SigmaDSP™ 3-Channel, 26-Bit Signal Processing DAC*

High Performance Multichannel Audio Codecs and DACs

There are many applications in DVD, audio, automotive, home theater, etc., where high performance multichannel codecs and DACs are required. The AD1839A (Reference 8) is one example of a high-end codec with 2 ADCs and 6 DACs. A simplified block diagram is shown in Figure 8.72.

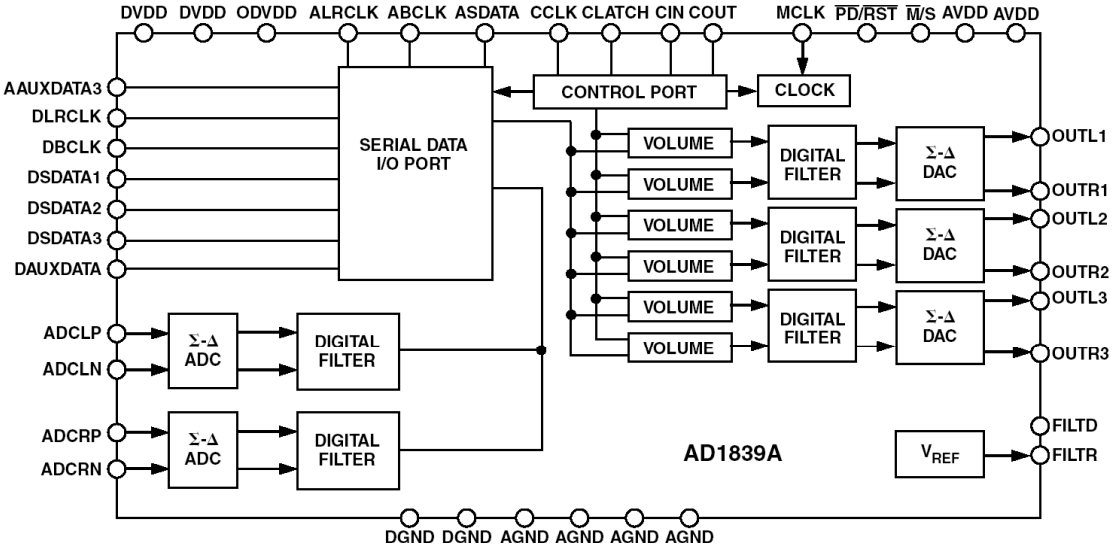


Figure 8.72: *AD1839A, 2 ADC, 6 DAC, 96-kSPS 24-Bit Σ-Δ Codecs*

The ADCs have 97-dB THD + N and 105-dB SNR/DNR. The DACs have 92-dB THD + N and 108-dB SNR/DNR. The devices operate on 5 V with 3.3-V tolerant digital interfaces. The maximum sampling rate is 96 kSPS (192 kSPS available on 1 DAC), and 16-/20-/24-bit word lengths are supported. The Σ-Δ modulators are multibit and utilize data directed scrambling. The AD1839A is housed in a 52-lead MQFP package.

A summary of the multichannel audio family of codecs and DACs is shown in Figure 8.73.

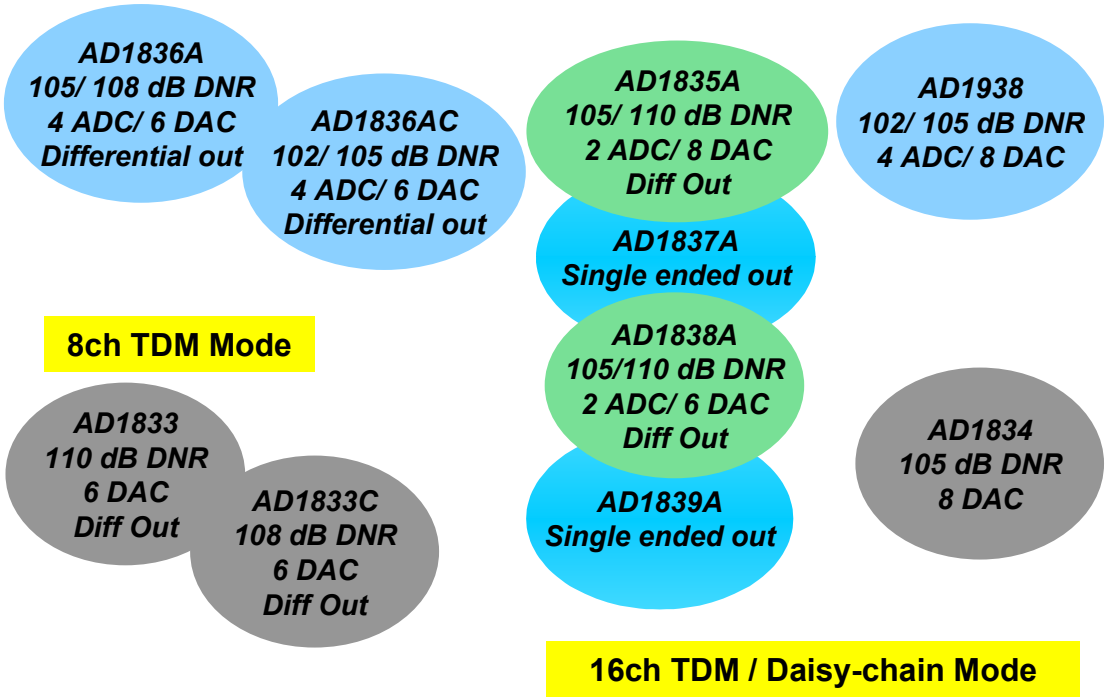


Figure 8.73: *Multichannel Audio Codecs and DACs*

There are many applications for audio codec products in computer sound cards, and these require compatibility with the AC'97 specification. The Analog Devices' AD1985 SoundMAX® Codec (Reference 9) is a good example of a codec which is compliant with the latest revision of AC'97.

Sample Rate Converters

From an earlier discussion in this section, we saw that there are a variety of standard sampling frequencies associated with digital audio signal processing: 8 kSPS, 32 kSPS, 44.1 kSPS, 48 kSPS, 88.2 kSPS, 96 kSPS, and 192 kSPS, etc. A typical audio studio generally has a common mixing console through which all signals must pass—analog audio and digital audio. These signals must be synchronized, and the most common method is to reference all signals to a 48 kHz master clock as shown in Figure 8.74. It should be noted that there are many other sample rate translations which might be required, with inputs and outputs ranging from 8 kSPS to 192 kSPS.

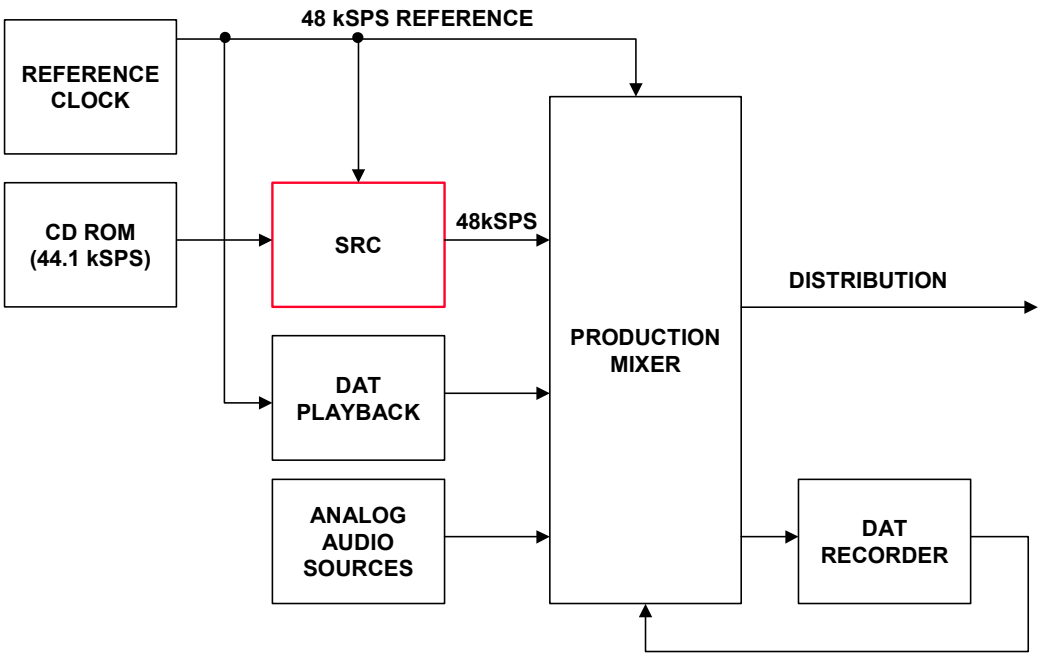


Figure 8.74: *The Need for Sample Rate Converters (SRCs)*

In order for this to be practical, there must be an easy method for seamlessly translating digital signals from one sampling frequency to another. For instance, the 44.1-kSPS CD player output must be translated into 48 kSPS to interface with the mixer. This requires more than simply changing the sampling frequency—a completely new set of data samples must be generated where these translations occur. Figure 8.75 shows one way to illustrate the concept of a sample rate converter (SRC).

- **A SRC is a FULLY DIGITAL ENGINE !!!**
- **However, one way of thinking about it is:**
  - **it reconstructs the signal, just like a DAC would do**
  - **it resamples the signal, just like an ADC would do**

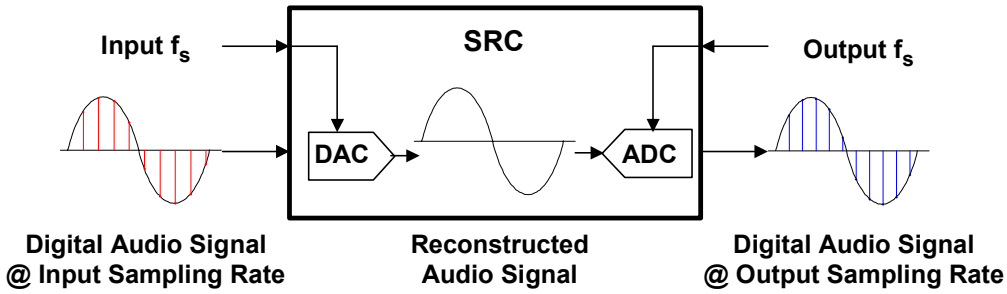


Figure 8.75: *The Concept of a Sample Rate Converter*

The digital input data is first passed through a DAC updated at the input sampling frequency. The analog output of the DAC is resampled by an ADC which operates at the output sampling frequency. In practice, however, the SRC is an entirely digital device. The process is conceptually one of upsampling the input data followed by zero-stuffing, digital interpolation to generate new sampled data, digital filtering, and finally downsampling to the desired output sampling frequency. The conversion of a 5-kHz sinewave from a sampling frequency of 44.1 kSPS to 48 kSPS using this technique is shown graphically in Figure 8.76.

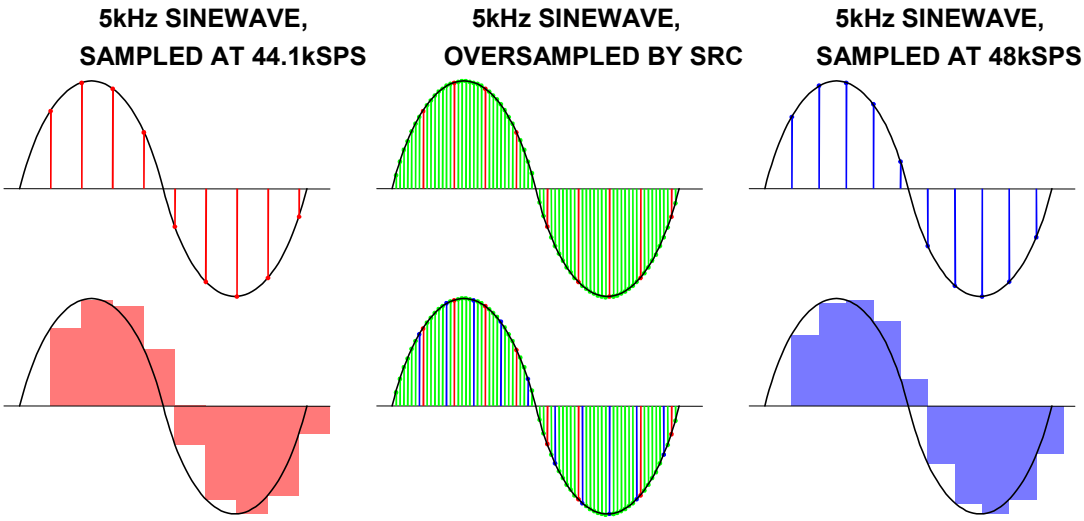


Figure 8.76: *Conversion of a 5-kHz Sinewave from 44.1-kSPS to 48-kSPS Sample Rate*

The AD1896 (Reference 10) is a 24-bit, high performance, single-chip, second generation asynchronous sample rate converter. Based on Analog Devices experience with its first asynchronous sample rate converter, the AD1890, the AD1896 offers improved performance and additional features. This improved performance includes a THD + N range of 117 dB to 133 dB, depending on the sample rate and input frequency, 142 dB (A-Weighted) dynamic range, up to 192-kSPS sampling frequencies for both input and output sample rates, improved jitter rejection, and 1:8 upsampling and 7.75:1 downsampling ratios.

Additional features include more serial formats, a bypass mode, better interfacing to digital signal processors, and a matched-phase mode. The AD1896 has a 3-wire interface for the serial input and output ports that supports left-justified, I^2S, and right-justified (16-, 18-, 20-, 24-bit) modes. Additionally, the serial output port supports TDM mode for daisy-chaining multiple AD1896s to a digital signal processor. The serial output data is dithered down to 20, 18, or 16 bits when 20-, 18-, or 16-bit output data is selected. The AD1896 sample rate converts the data from the serial input port to the sample rate of the serial output port. The sample rate at the serial input port can be asynchronous with respect to the output sample rate of the output serial port. The master clock to the AD1896, MCLK, can be asynchronous to both the serial input and output ports.

The AD1896 operates on 3.3-V to 5-V input supplies and 3.3-V core voltages. The part is housed in a 28-lead SSOP package. A functional diagram is shown in Figure 8.77.

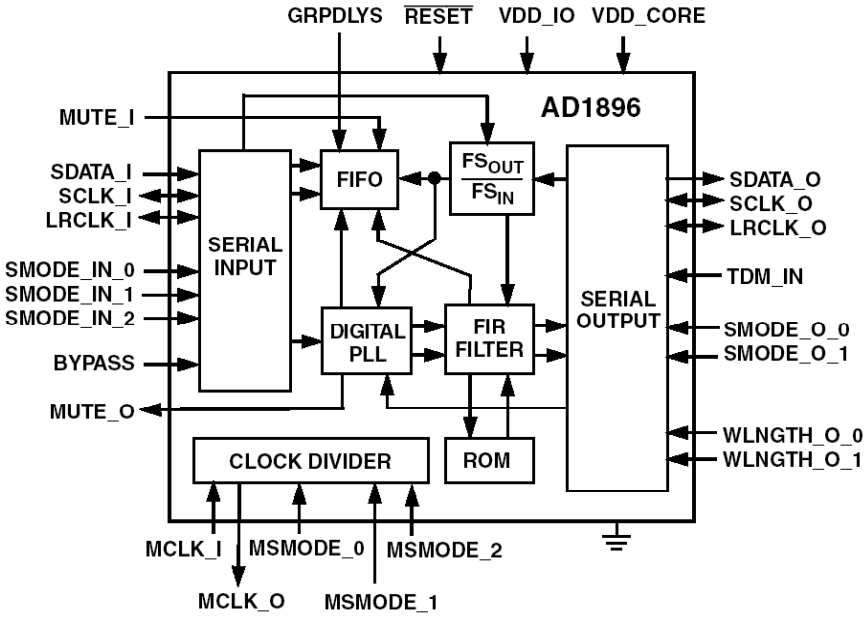


Figure 8.77: *AD1896 192-kHz Stereo Asynchronous Sample Rate Converter*

REFERENCES:
8.4 DIGITAL AUDIO

1. Alec Harley Reeves, "Electric Signaling System," **U.S. Patent 2,272,070**, filed November 22, 1939, issued February 3, 1942. Also **French Patent 852,183** filed 1937, issued 1938, and **British Patent 538,860** issued 1939.

2. L. A. Meacham and E. Peterson, "An Experimental Multichannel Pulse Code Modulation System of Toll Quality," **Bell System Technical Journal**, Vol 27, No. 1, January 1948, pp. 1-43.

3. Michael Robin and Michel Poulin, **Digital Television Fundamentals**, Second Edition, McGraw-Hill, 2000, ISBN 0-07-135581-2, Chapter 6.

4. Data sheet for AD74122 16-/20-/24-Bit, 48-kSPS Stereo Voiceband/Audio Codec, http://www.analog.com.

5. Data sheet for AD1871 Stereo Audio, 24-Bit, 96-kSPS, Multibit Σ-Δ ADC, http://www.analog.com

6. Data sheet for AD1955 High Performance Multibit Σ-Δ DAC, http://www.analog.com.

7. Data sheet for AD1953 SigmaDSP™ 3-Channel, 26-Bit Signal Processing DAC, http://www.analog.com.

8. Data sheet for AD1839A 2 ADC, 6 DAC, 96-kSPS 24-Bit Σ-Δ Codecs, http://www.analog.com.

9. Data sheet for AD1985 AC'97 SoundMAX® Codec, http://www.analog.com.

10. Data sheet for AD1896 192-kSPS Stereo Asynchronous Sample Rate Converter, http://www.analog.com.

11. Ken C. Pohlmann, **Principles of Digital Audio**, Fourth Edition, McGraw Hill, 2000, ISBN 0-07-134819-0.

SECTION 8.5: DIGITAL VIDEO AND DISPLAY ELECTRONICS

Walt Kester

Digital Video

Introduction

Before discussing some video applications for data converters, we will review some basics regarding video signals and specifications. The standard video format is the specification of how the video signal looks from an electrical point of view. Light strikes the surface of an image sensing device within the camera, producing a voltage level corresponding to the amount of light hitting a particular spatial region of the surface. This information is then placed into the standard format and sequenced out of the camera. Along with the actual light and color information, synchronization pulses are added to the signal to allow the receiving device—a television monitor, for instance—to identify where the sequence is in the frame data.

A standard video format image is read out on a line-by-line basis from left to right, top to bottom. A technique called *interlacing* refers to the reading of all even numbered lines, top to bottom, followed by all odd lines as shown in Figure 8.78.

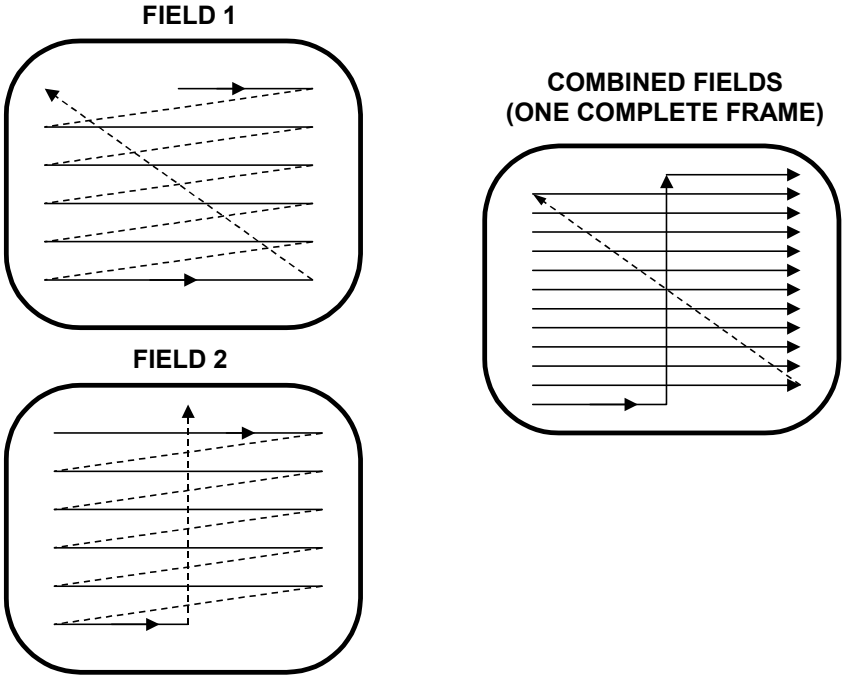


Figure 8.78: *Standard Broadcast Television Interlace Format*

The standard television picture *frame* is thus divided into even and odd *fields*. Interlacing is used to produce an apparent update of the entire frame in half the time that a full update actually occurs. This results in a television image with less apparent flicker. Typical broadcast television frame update rates are 30 Hz and 25 Hz, depending upon the line frequency. It should be noted that interlacing is generally not used in graphics display systems where the refresh rate is usually greater (typically 60 Hz).

The original black and white, or *monochrome*, television specification in the USA is the EIA RS-170 (replaced by SMPTE 170M) specification that prescribes all timing and voltage level requirements for standard commercial broadcast video signals. The standard American specification for color signals, NTSC, modifies RS-170 to work with color signals by adding color information to the signal which otherwise contains only brightness information.

A video signal comprises a series of analog television lines. Each line is separated from the next by a synchronization pulse called the *horizontal sync*. The fields of the picture are separated by a longer synchronization pulse, called the *vertical sync*. In the case of a monitor receiving the signal, its electron beam scans the face of the display tube with the brightness of the beam controlled by the amplitude of the video signal. A single line of an NTSC color video signal is shown in Figure 8.79.

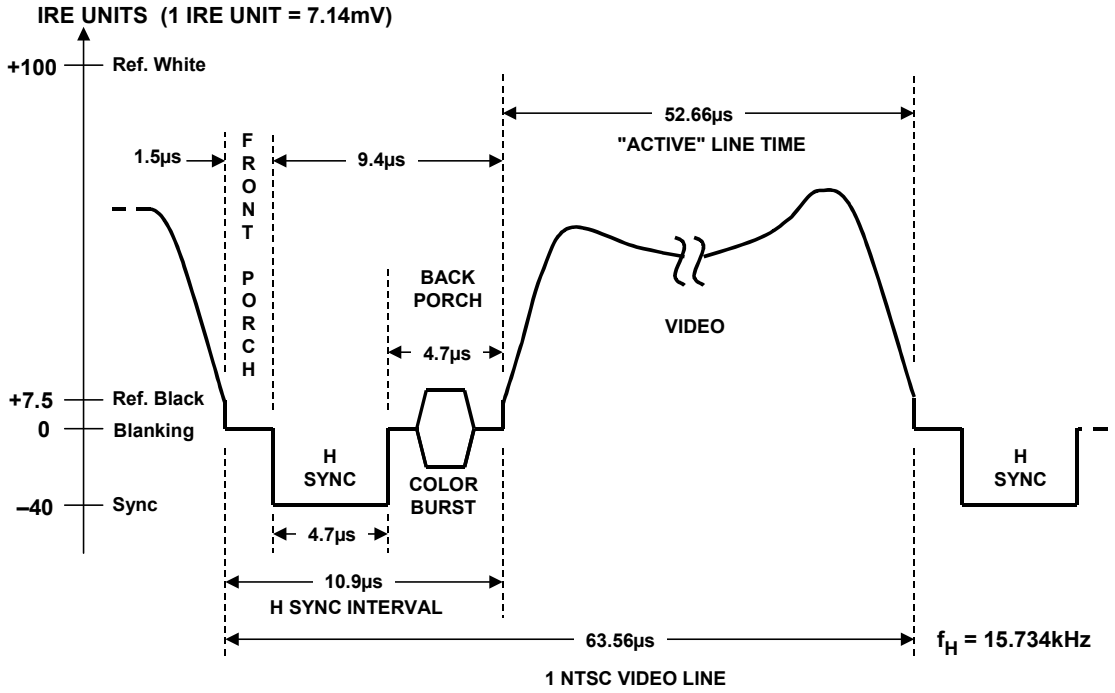


Figure 8.79: *NTSC Composite Color Video Line*

Whenever a horizontal sync pulse is detected, the beam is reset to the left side of the screen and moved down to the next line position. A vertical sync pulse, indicated by a horizontal sync pulse of longer duration, resets the beam to the top left point of the screen to a line centered between the first two lines of the previous scan. This allows the current field to be displayed between the previous one.

In the NTSC system (used in the U.S. and Japan), the color subcarrier frequency is 3.58 MHz. The PAL system (used in the U.K. and Germany) and SECAM system (used in France) use a 4.43-MHz color subcarrier.

In terms of their key frequency differences, a comparison between the NTSC system and the PAL system are given in Figure 8.80.

	NTSC	PAL
Horizontal Lines	525	625
Color Subcarrier Frequency	3.58MHz	4.43MHz
Frame Frequency	30Hz	25Hz
Field Frequency	60Hz	50Hz
Horizontal Sync Frequency	15.734kHz	15.625kHz

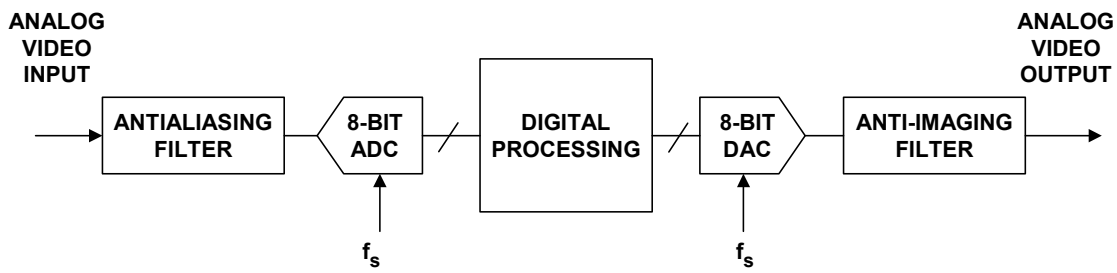
Figure 8.80: *NTSC and PAL Signal Characteristics*

Digital Video Formats

Digital video had its beginnings in the early 1970s when 8-bit ADCs with sampling frequencies of 15 MSPS to 20 MSPS became available. Subjective tests, such as those conducted by A. A. Goldberg (Reference 1) showed that 8-bit resolution was sufficient for digitizing the composite video signal at sampling frequencies of 3 or 4 times the NTSC color subcarrier frequency (3.58 MHz).

Digital techniques were first applied to "video black boxes" which replaced functions previously implemented using analog techniques. These early digital black boxes had an analog video input and an analog video output, and replaced analog-based equipment such as time-base correctors, frame stores, standards converters, etc. (Reference 2, 3, 4). A typical black box is shown in Figure 8.81.

As previously mentioned, the required resolution was determined to be 8-bits early in the 1970s, however, 9-bit and 10-bit resolution eventually became popular as higher resolution low-cost ADCs and DACs became available. Some initial black boxes used sampling frequencies of 3 times the subcarrier frequency—simply due to the lack of faster ADCs, but ultimately 4 times the subcarrier frequency became the industry standard.



COMPOSITE VIDEO SIGNAL CHARACTERISTICS

	BANDWIDTH	SUBCARRIER, f_{SC}	$f_s = 3\ f_{SC}$	$f_s = 4\ f_{SC}$
NTSC	4.2 MHz	3.58 MHz	10.74 MSPS	14.32 MSPS
PAL	5.0 MHz	4.43 MHz	13.29 MSPS	17.72 MSPS

Figure 8.81: *Digital Video "Black Box"*

The early ADCs used in these digital block boxes were modular devices, however in 1979, the first commercial 8-bit monolithic flash converter was introduced (Reference 5), and within a few years was soon followed by many others from a variety of IC manufacturers. The availability of low-cost IC ADCs played a large role in the growth of digital video.

Digital videotape recorders (VTRs) emerged in the 1980s, based on CCIR recommendations. More digital black boxes proliferated, such as digital effects generators, graphic systems, and still stores—these devices operating in a variety of noncorrelated and incompatible standards. Digital connections between the black boxes were difficult or impossible, and the majority were connected with other equipment using analog input and output ports. As a matter of fact, this was one reason why 9-bit and 10-bit ADCs became popular—the additional resolution reduced the cumulative effects of quantization noise in cascaded devices.

In the 1980s, the Society of Motion Picture and Television Engineers (SMPTE) developed a digital standard (SMPTE 244M, Reference 6) which defined the characteristics of $4f_{SC}$ sampled NTSC composite digital signals as well as the characteristics of a bit-parallel digital interface which allowed up to 10-bit samples. The digital interface consisted of 10 differential ECL-compatible data signals, 1 differential ECL-compatible clock signal, 2 system grounds, and 1 chassis ground, for a total of 25 pins. Also in the 1980s, an IEEE standard (Reference 7) was developed which defined test methods for measuring the performance of ADCs and DACs used in composite digital television applications. Later, digital systems using $4f_{SC}$ NTSC composite digital signals adopted a high-speed bit-serial interface, with a data rate of 143 Mb/s (defined in SMPTE 259M, Reference 10).

Even before the finalization of the $4f_{SC}$ composite digital standard, work was progressing on digital *component* systems, which offer numerous advantages over the composite digital systems. To understand the differences and advantages, Figure 8.82 shows a generalized block diagram of how the composite broadcast video signal is constructed.

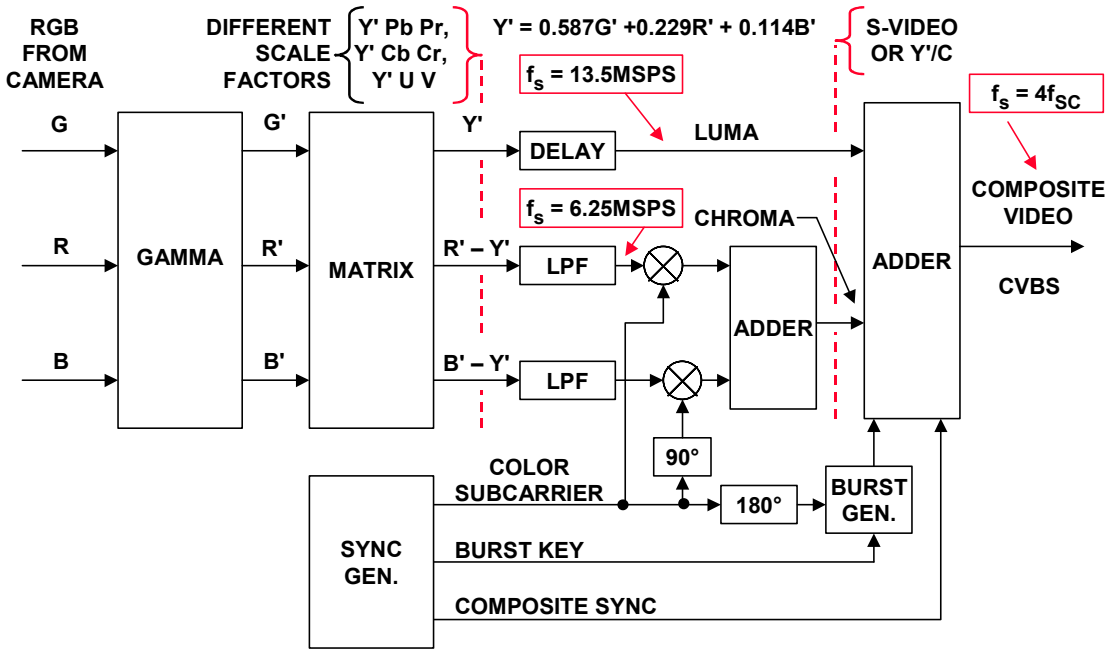


Figure 8.82: *Model for Generating the Composite Video Signal from RGB Components*

The native RGB signals from the color camera are first passed through a nonlinear *gamma* unit which compensates for the inherent nonlinearity in the receiving CRT. The R'G'B' outputs of the gamma unit then pass through a resistive *matrix* which generates a high-bandwidth *luma* signal (often incorrectly called *luminance*) and two reduced-bandwidth color difference signals. The luma signal, Y', is formed using the relationship Y' = 0.587G' + 0.229R' + 0.114B'. In addition, two *color difference* signals, designated R' – Y' and B' – Y' are formed. The color subcarrier is then used to modulate the color difference signals in quadrature, and they are summed to form the *chroma* signal (often incorrectly called *chrominance*). The color burst and composite sync signals are then combined with the luma and chroma signals to form the *composite* video signal, designated CVBS (composite video with burst and sync)—the composite signal is ultimately broadcast.

A reverse process occurs in the television receiver, where the composite signal is decomposed into the various components and finally into an RGB signal which ultimately drives the three color inputs to the CRT.

Note that each step in the construction of the composite video signal after the output of the resistive matrix has the potential of introducing artifacts in the signal. For this reason, engineers working in digital video soon realized that it would be advantageous to keep the digital video signal as close to the native R'G'B' format as possible. The first so-called *component* analog video standard developed was designated as *Y'PbPr* (note that the prime notation has been dropped from most modern nomenclature). The corresponding

digital standard is designated *Y'CbCr*. Digital Y'CbCr component video is specified in References 8, 9, and 10.

Another analog component standard is designated as Y'UV and is similar to Y'PbPr with different scaling factors for the color difference signals.

The final popular analog component standard to be discussed is the so-called *S-Video*, or simply *Y'/C*. This is a two-component analog system and is often used in high-end VCRs, DVDs, and TV receivers and monitors.

The various analog digital video component standards are summarized in Figure 8.83, and the back panel connections for each are shown in Figure 8.84 for a typical high-end video receiver.

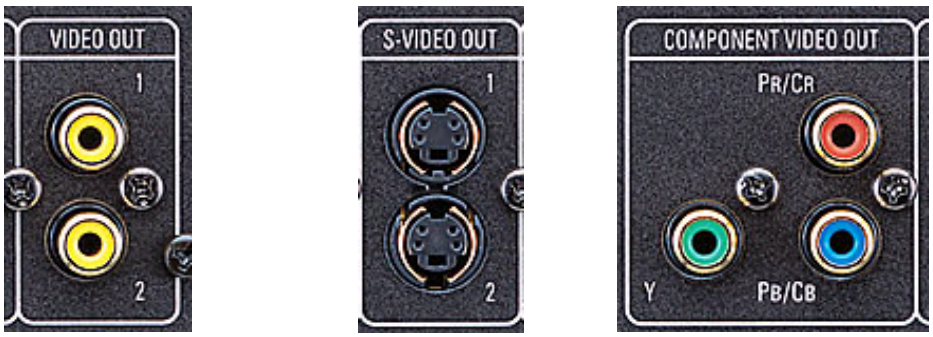
- **Y'PbPr**
  - **In component *analog* video, B' – Y' and B' – Y' scaled to form color difference signals Pb and Pr.**
- **Y'CbCr**
  - **In component *digital* video, B' – Y' and B' – Y' scaled to form Cb and Cr components.**
- **Y'UV**
  - **In NTSC or PAL, B' – Y' and B' – Y' scaled to form U and V *analog* components. U and V are lowpass filtered, and combined into a modulated chroma component, C. Luma (Y) is summed with chroma to form composite NTSC or PAL signal.**
- **S-Video, or Y'/C**
  - ***Analog* two-component system based on luma (Y') and chroma (C) signals.**
- **Composite, or CVBS**
  - **Composite video signal with burst and sync.**

Figure 8.83: *Analog and Digital Video Component and Composite Standards*

The digital component video standards (References 8, 9, and 10) call for a sampling frequency of 13.5 MSPS for the Y' luma signal and 6.25 MSPS for each of the two color difference signals, Pb and Pr. This is often referred to as "4:2:2 sampling." The luma sampling frequency of 13.5 MSPS was selected to allow an integer number of sample periods in the line periods in both NTSC and PAL standards.

The 13.5-MSPS standard is sufficient for the luma signal whose bandwidth extends to 5.75 MHz. The color difference signal bandwidths extend to 2.75 MHz, and the 6.25-MSPS is also adequate.

It should be noted that if the R'B'G' signals were sampled directly, each would require a sampling frequency of 13.5 MSPS, and this is referred to as "4:4:4 sampling."



CVBS Composite Video with Burst and Sync	S-Video Y'/C	Component Video Y'PrPb or Y'CrCb
2 Outputs	2 Outputs	1 Output

Figure 8.84: *What the Analog Connectors Look Like on a High-End Receiver*

Serial Data Interfaces

Because of the large number of digital interconnection lines required with parallel interfaces, the serial digital interface (SDI) has mostly replaced the early parallel interfaces. The current serial interface standard is SMPTE 259M (Reference 10) defines 10-bit serial interfaces for $4f_{SC}$ NTSC at about 143 Mb/s, $4f_{SC}$ PAL at about 177 Mb/s, ITU-R BT601 4:2:2 component video at 270 Mb/s, ITU-R BT601 4:2:2 component video sampled at 18 MSPS (to achieve 16:9 aspect ratio) at 360 Mb/s.

High definition TV (HDTV) standards with a 16:9 aspect ratio are defined in ITU-R BT709 (Reference 12) and SMPTE 292M (Reference 13). A sampling frequency of 74.25 MSPS is used with 4:2:2 component sampling, for a serial bit rate of 1.485 Gb/s. There are various other HDTV scanning standards which are defined in SMPTE 296M and SMPTE 274M.

The high data rates associated with digital television require the use of data compression (such as MPEG) for broadcast transmission, but within the studio the signals are typically transmitted in serial uncompressed format on either coaxial or fiber optic cable.

The field of digital television is somewhat complicated because of the large number of acronyms and standards. For further information, the reader should consult References 14 and 15.

Digital Video ADCs and DACs: Decoders, and Encoders

In the world of digital video, a few definitions are in order. The acronym SDTV simply refers to standard definition TV (as opposed to HDTV, high definition TV).

An SDTV *decoder* converts *analog* composite video (CVBS), S-Video (Y'/C), Y'UV, or Y'PbPr signals into a digital video steam in the form of a Y'CbCr digital stream per ITU-R BT.656 4:2:2 component video compatible with NTSC, PAL B/D/G/H/I/ PAL M, or PAL N. An ADC function is implicit in the definition of the video decoder, but traditionally, the term decoder is more generally used to define the DAC function.

A digital video *encoder* converters digital component video (ITU-R BT.601 4:2:2, for example) into a standard composite analog baseband signal compatible with NTSC, PAL B/D/G/H/I, PAL M, or PAL N. In addition to the composite output signal, there is often the facility to output S-Video (Y'/C), RGB, Y'PbPr, or Y'UV component analog video.

In contrast to the digital video terminology, in ADC and DAC terminology, the terms *encoder* and *decoder* are used to refer to the ADC and the DAC function, respectively, and the combination is called a *codec* (coder-decoder).

The reason for this is that video engineers consider a composite color signal to have the chroma *encoded* on top of the luma signal. The video *decoder* (with the ADCs) *decodes* (separates) the chroma and luma signal and is referred to as the *decoder*. On the other hand, the video *encoder encodes* the chroma and the luma back into the composite signal.

The first ADCs and DACs used in digital television in the 1970s were modular devices, and were typically 8-bits with $4f_{SC}$ sampling, requiring an upper sampling rate of 17.72 MSPS for PAL. Many of the digital video black boxes of the 1980s ultimately went to 9-and even 10-bit resolution when IC ADCs became available. The analog conditioning circuitry, such as clamping, dc restoration, and filtering was typically separate from the ADC function itself.

In the 1990s, many low-cost CMOS ADCs and DACs became available with resolutions up to 12-bits, and sampling rates of greater than 20 MSPS, thereby solving the basic data conversion problem and paving the way for higher levels of mixed-signal integration. Modern video decoders and encoders are therefore highly integrated, with on-chip analog signal conditioning and digital signal processing. Video decoders and encoders may operate at typical sampling frequencies of $4f_{SC}$, 13.5 MSPS, 27 MSPS, 54 MSPS, 108 MSPS, 216 MSPS, or 74.25 MSPS.

The ADV7183A 10-bit video decoder (Reference 16) is a good example of a modern highly integrated video signal processor, and a simplified block diagram is shown in Figure 8.85.

The ADV7183A is an integrated video *decoder* that automatically detects and converts a standard definition analog baseband television signal (SDTV) compatible with worldwide standards NTSC , PAL, or SECAM into 4:2:2 component video data compatible with 16-/8-bit ITU-R BT.601/ITU-R BT.656. The advanced and highly flexible digital output interface enables high performance video decoding and conversion in both frame-buffer-based and line-locked clock-based systems. This makes the device ideally suited for a broad range of applications with diverse analog video characteristics, including tape-based sources, broadcast sources, security/surveillance cameras, and professional systems.

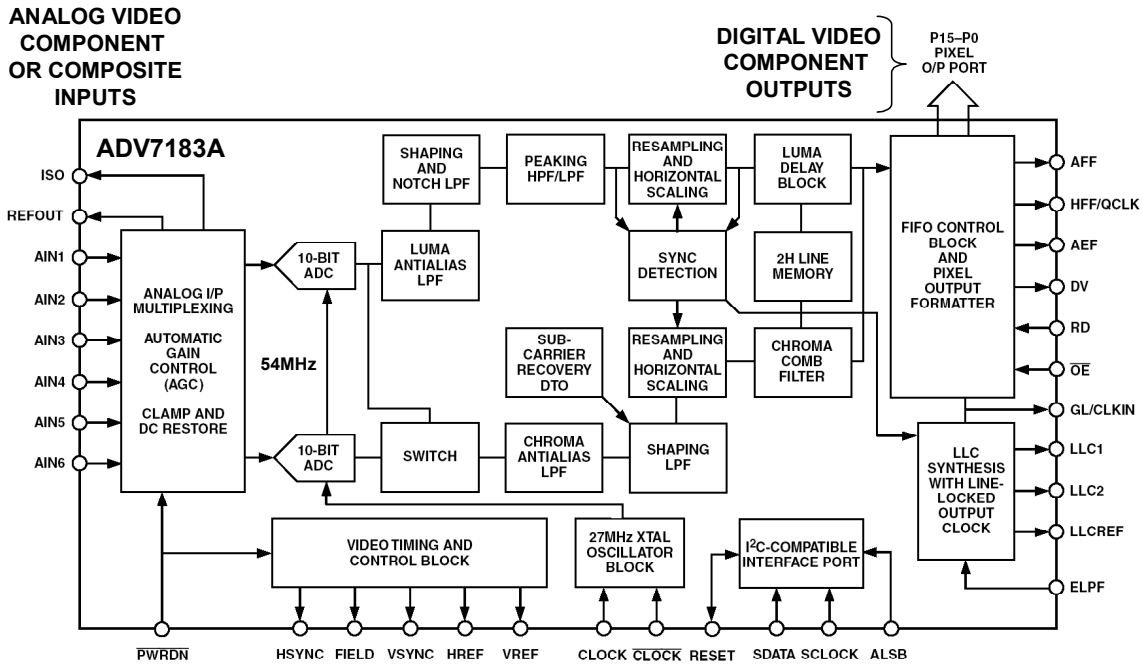


Figure 8.85: *ADV7183A 10-Bit Video Decoder*

The internal 10-bit accurate A/D conversion provides professional quality SNR performance. This allows true 8-bit resolution in the 8-bit output mode. The analog input channels accept standard composite (CVBS), S-video, and component Y'PrPb video signals in an extensive number of combinations. AGC and clamp restore circuitry allow an input video signal peak-to-peak range of 0.5 V up to 2 V. Alternatively, these can be bypassed for manual settings.

The fixed 54-MHz (4 × 13.5 MSPS) clocking of the ADCs and data path for all modes allows very precise and accurate sampling and digital filtering. The line-locked clock output allows the output data rate, timing signals, and output clock signals to be synchronous, asynchronous, or line-locked even with ±5% line length variation. The output control signals allow glueless interface connection in almost any application. The ADV7183A modes are set up over a 2-wire serial bi-directional port (I^2C-compatible). The ADV7183A is fabricated in a +3.3-V CMOS process. Its monolithic CMOS construction ensures greater functionality with lower power dissipation. The ADV7183A is packaged in a small 80-pin LQFP package.

The ADV7310 (Reference 17) is a second generation 12-bit video *encoder* featuring high performance DACs using oversampled Noise Shaped Video (NSV™) techniques to achieve better levels of performance for mid-range consumer electronics and professional video solutions. The maximum sampling rate is 216 MSPS which enables up to 16× oversampling. This means better figures for differential gain, phase and signal to noise ratio. A simplified block diagram of the ADV7310 is shown in Figure 8.86.

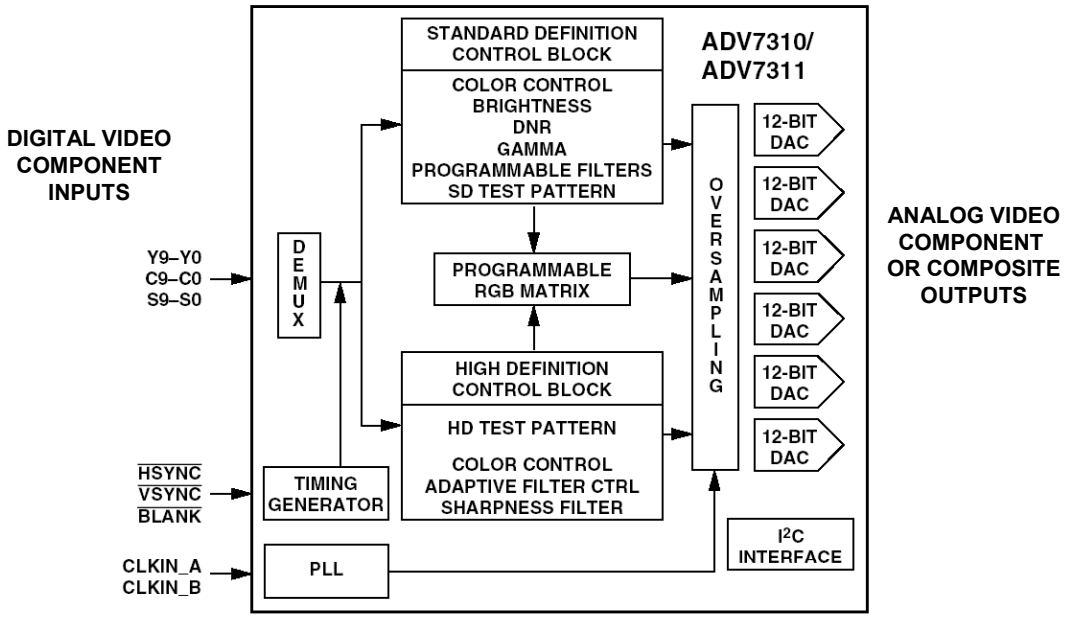


Figure 8.86: *ADV7310 Multi-Format 216-MSPS Video Encoder*

The ADV7310 accepts a variety of standard digital video component input formats, including HDTV and SDTV. Outputs are HDTV, SDTV component and composite, S-Video, etc. Six 12-bit NSV precision video DACs provide multiple video outputs and allows 2×, 4×, 8× and 16× oversampling for high definition, progressive scan and standard definition video. A DAC adjust feature allows fine tuning of output levels on analog interfaces internal to many items of equipment, especially TVs, where EMI compliance requirements can be tough to meet.

The ADV7310 has a standard 2-wire serial I^2C-compatible interface, and is housed in a 64-lead LQFP package.

Specifications for Video Decoders and Encoders

Video decoders and encoders are generally specified in terms of video performance, in addition to some of the traditional ADC/DAC specifications. Figure 8.87 lists the typical video specifications, and their definitions can be found in Reference 7, 14, and 15.

- **Resolution, Sampling Rate, Linearity, Bandwidth**
- **Differential Gain (CVBS)**
- **Differential Phase (CVBS)**
- **SNR**
- **Chroma-Specific (Component Video)**
  - **Hue Accuracy**
  - **Color Saturation Accuracy**
  - **Color Gain Control Range**
  - **Analog Color Gain Range**
  - **Digital Color Gain Range**
  - **Chroma Amplitude Error**
  - **Chroma Phase Error**
  - **Chroma/Luma Intermodulation**
- **Luma-Specific (Component Video)**
  - **Luma Brightness Accuracy**
  - **Luma Contrast Accuracy**

Figure 8.87: *Video Decoder and Encoder Specifications*

Note that the differential gain and differential phase specifications (defined in Chapter 2 and 5 of this book) apply only to the composite video signal and not the component video signals.

Display Electronics

Manufacturers of computer graphics displays realized that the resolution provided by standard NTSC and PAL video monitors was not sufficient for serious computer users because of the close viewing distance required. They also realized that the best performance could be obtained by utilizing the native RGB component video rather than composite signals.

For these reasons, a variety of formats for resolution/scanning standards have evolved, generally defined by the somewhat obsolete EIA RS-343A standard. Unlike broadcast video, the horizontal and vertical resolution as well as the refresh rate in a graphics display system can vary widely depending upon the desired performance. The resolution in such a system is defined in terms of *pixels* based on the number of horizontal lines and the number of pixels in each line. For instance, a 640 × 480 monitor has 480 horizontal lines, and each horizontal line is divided into 640 pixels. So a single frame would contain 307,200 pixels. In a color system, each pixel requires RGB intensity data. This data is generally stored as 8- or 10-bit words in a memory. Refresh rates generally vary from

60 Hz to 85 Hz. Most modern raster scan computer graphics monitors are "multisync," i.e, they will automatically synchronize to a variety of refresh rates and resolutions.

Figure 8.88 shows some typical resolutions and pixel rates for common display systems, assuming a 75-Hz, non-interlaced refresh rate. Standard computer graphics monitors, like television monitors, use a display technique known as *raster scan*. This technique writes information to the screen line by line, left to right, top to bottom, as has been previously discussed. The monitor must receive a great deal of information to display a complete picture. Not only must the intensity information for each pixel be present in the signal but information must be provided to determine when a new line needs to start (HSYNC) and when a new picture frame should start (VSYNC).

NOTATION	RESOLUTION	REFRESH RATE	PIXEL RATE
VGA	640 × 480	75Hz	30MHz
SVGA	800 × 600	75Hz	47MHz
XGA	1024 × 768	75Hz	83MHz
SXGA	1280 × 1024	75Hz	138MHz
UXGA	1600 × 1200	75Hz	202MHz
QXGA	2048 × 1536	75Hz	330MHz

Pixel Rate ≈ Vertical Resolution × Horizontal Resolution × Refresh Rate × 1.4
Refresh rates can be from 60Hz to 100Hz

Figure 8.88: *Typical Graphics Resolution and Pixel Rates for 75-Hz Non-Interlaced Refresh Rate*

The pixel clock frequency gives a good idea of the settling time and bandwidth requirements for any analog component, such as the DAC, which is placed in the path of the RGB signals. The pixel clock frequency can be estimated by finding the product of the horizontal resolution times the vertical resolution times the refresh rate. An additional 40% should be added, called the retrace factor, to allow for overhead.

There are several system architectures which may be used to build a graphics display system. The most general approach is illustrated in Figure 8.89. It consists of a host microprocessor, a graphics controller, a video frame buffer, three color memory banks (lookup tables), one for each of the primary colors red, green, and blue, (only one for monochrome systems). The microprocessor provides the image information to the graphics controller, frame buffer, and to the color lookup tables. This information typically includes position and color information. The graphics controller is responsible for interpreting this information and adding the required output signals such as sync, blanking, and memory management signals. The high speed frame buffer provides pixel address information to the lookup tables at the pixel rate.

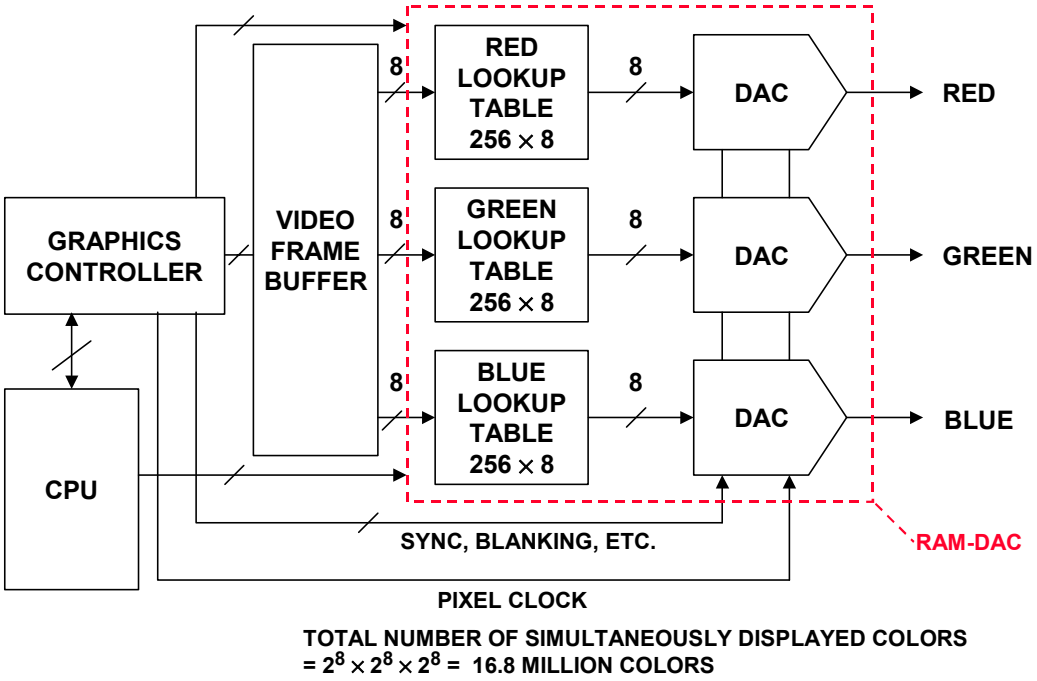


Figure 8.89: *Simplified Graphics Control System for Generating RGB Signals*

The R, G, and B memories are therefore lookup tables which hold the intensity information for each pixel for one frame . The DACs use the words in the memory and information from the memory controller to write the pixel information to the monitor. This system, when used with 8-bits for each DAC, is known as a 24-bit "true color" system. A total of 16.8 million addressable colors can be displayed simultaneously. The lookup tables and the DACs are generally integrated into an IC called a video "RAM-DAC," thereby minimizing the memory requirements of the graphics controller. Once the data for a frame is loaded into the RAM-DAC, no more data is required from the graphics controller unless there is a change in the pixel content.

In an effort to reduce system costs while maintaining flexibility, an alternative configuration shown in Figure 8.90 was developed, called a "pseudo-color" 8-bit graphics system. In this configuration, only 256 individuals colors out of the total of 16.8 million can be displayed simultaneously, which is often acceptable in low-end applications. Today, most graphics controllers are capable of providing 8-bit ("256 color"), 16-bit ("high color"), and 24-bit ("true color") outputs.

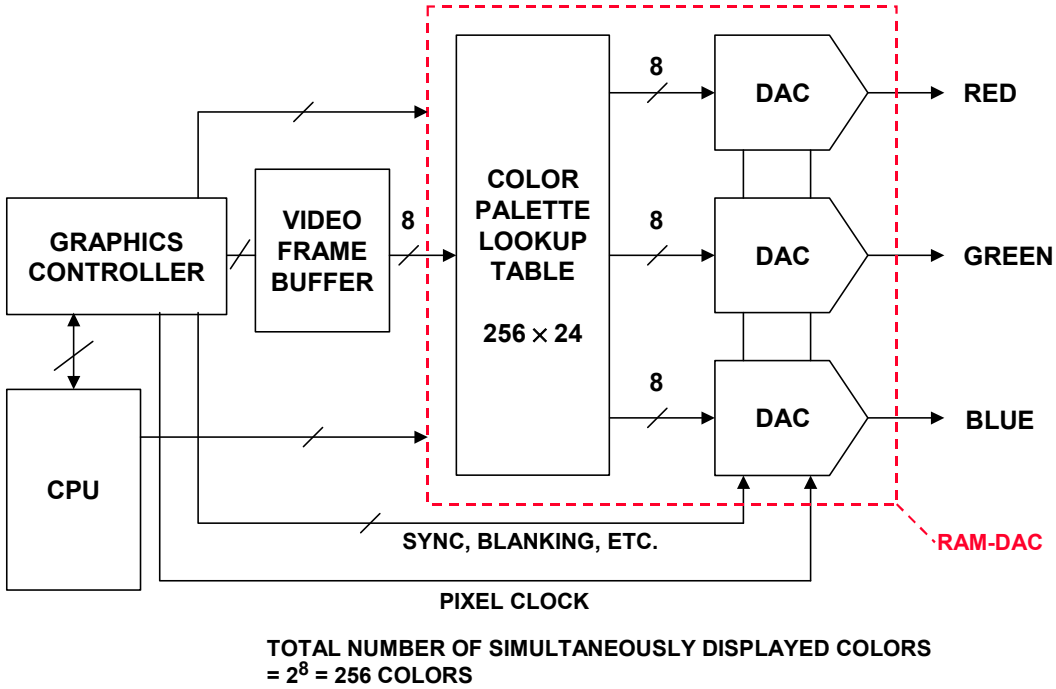


Figure 8.90: *"Pseudo-Color" 8-Bit RGB Graphics System*

Video DACs have some features which distinguish them from traditional high speed DACs. Figure 8.91 shows the output waveform and levels for the green output which contains the sync information. Notice that the current output video DAC is terminated by a 75-Ω resistor to ground (source termination), and the end of the 75-Ω cable is terminated with another 75-Ω resistor (load termination). The net dc load on the output of the DAC is therefore 37.5 Ω. In order to develop a fullscale 1-V output, a current output of 26.67 mA is required for the green output DAC. In a graphics system, 1 IRE unit corresponds to approximately 7 mV. Note that all 8-bits (256 levels) of the DAC are devoted to the active video region between the blanking level and the white level. The 300-mV sync level is generated by a separate current switch in the green DAC. A separate input is also supplied which generates the blanking level. In some systems, sync and blanking is applied to all three color signals, however it is very common practice to apply the sync signal to the green only (sync-on-green, or SOG).

Looking at high-end video DACs, the ADV7125 is a triple 330-MSPS DAC on a single monolithic chip (Reference 18). It consists of three high speed, 8-bit video DACs with complementary current outputs, a standard TTL input interface, and a high impedance analog current output. The ADV7125 has three separate 8-bit-wide input ports. A single 5-V or 3.3-V power supply and clock are all that are required to make the part functional. The ADV7125 has additional video control signals for composite SYNC and BLANK, as well as a power-save mode. The ADV7125 is fabricated in a 5-V CMOS process. Its monolithic CMOS construction ensures greater functionality with lower power dissipation (250 mW @ 3.3 V, 330 MSPS update). The ADV7125 is available in a 48-lead LQFP package. A simplified functional diagram is shown in Figure 8.92.

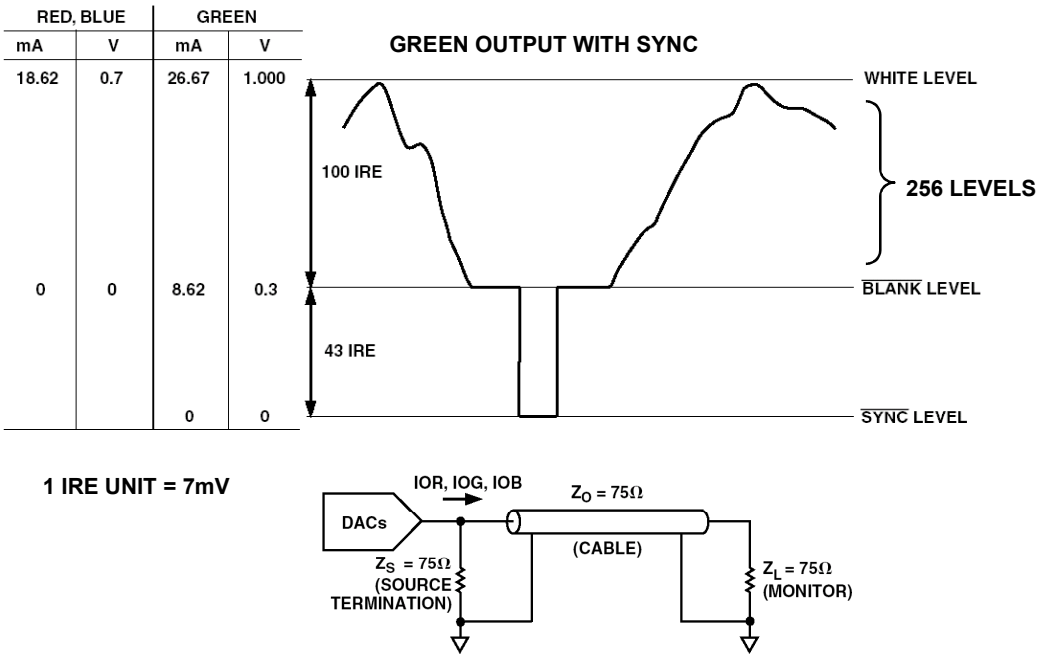


Figure 8.91: *Video Levels in RGB Graphics Displays*

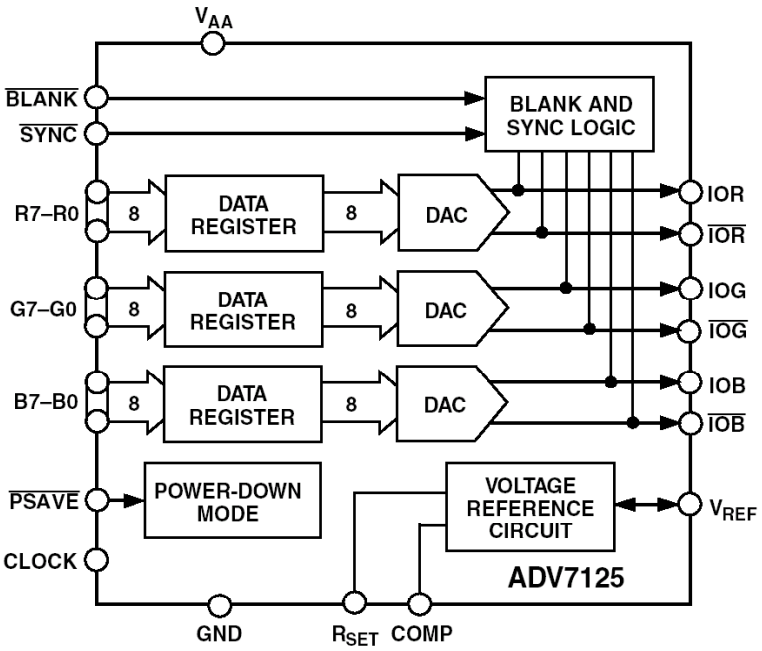


Figure 8.92: *ADV7125 330-MSPS Video DAC*

Today, there are a variety of video RAM-DACs which include the color lookup tables as well as the DACs, plus additional features such as overlay palettes and various mode controls. These digital features are integrated with the video DACs to provide a high degree of functionality. Figure 8.93 shows the ADV7160/ADV7162 true color, 220-MSPS video RAM-DAC (Reference 19).

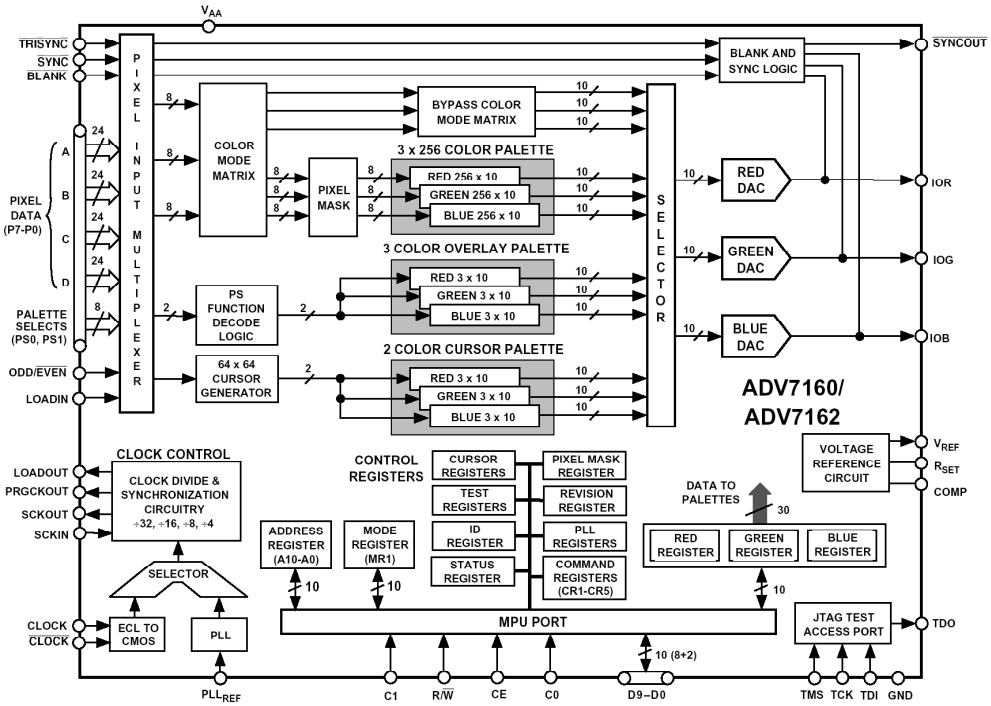


Figure 8.93: *ADV7160/ADV7162 220-MSPS Video RAM-DAC*

The ADV7160/ADV7162 has a 96-bit fully programmable pixel port for support of up to 220-MSPS 1600 × 1280 screen resolution at an 85-Hz refresh rate. The lookup tables are 10-bits, thereby allowing on-chip gamma correction. The device has a fully programmable on-board PLL, and a standard microprocessor I/O interface. The overlay palettes allow the addition of cursors, pull-down menus, grids, pointers, etc., without additional hardware or software overhead. By providing these limited depth overlay palettes, the system software, which is generally responsible for cursor and pointer control, menus, etc., can efficiently control these graphics without altering the main graphic image which is controlled by the application software.

The ADV7160/ADV7162 operates on a single +5-V supply and is housed in either a 160-lead thermally enhanced QPF PQUAD (ADV7160), or a 160-lead plastic quad flatpack QFP (ADV7162).

Flat Panel Display Electronics

The popularity of flat panel LCD-based displays has steadily increased over the last few years, and they are rapidly replacing CRT-based monitors in desktop computer systems. In addition, LCD projectors have virtually replaced 35-mm slide and overhead projectors as a means of delivering presentation material.

The graphics card in a typical desktop computer system converts the digital pixel data to an analog RGB signal for driving an external monitor. In a laptop computer the built-in LCD display is generally driven directly with the digital data, and it is also converted it to analog RGB video using video DACs, where it is available on an output connector for driving an external monitor or projector.

The analog RGB interface to the CRT is the primary workhorse in the display of computer-generated graphics data. A large legacy of PC-graphics adapters currently exist that use RAM-DACs to convert digital graphics data to analog RGB signals. The new flat panel displays must therefore be able to interface with this conventional technology to achieve market penetration and fast acceptance (References 20 and 21).

In an effort to establish an industry-wide standard for the next-generation flat panel displays, the Digital Display Working Group (DDWG) developed the Digital Video Interface (DVI 1.0) specification (Reference 22). This specification describes how designers should implement the analog and digital interfaces. Analog timing is described in the Video Electronics Standards Association (VESA) standard for monitors, and the digital interface uses Transistion Minimized Differential Signaling (TMDS) format.

The generalized analog interface between the PC graphics card and the flat panel display is shown in Figure 8.94.

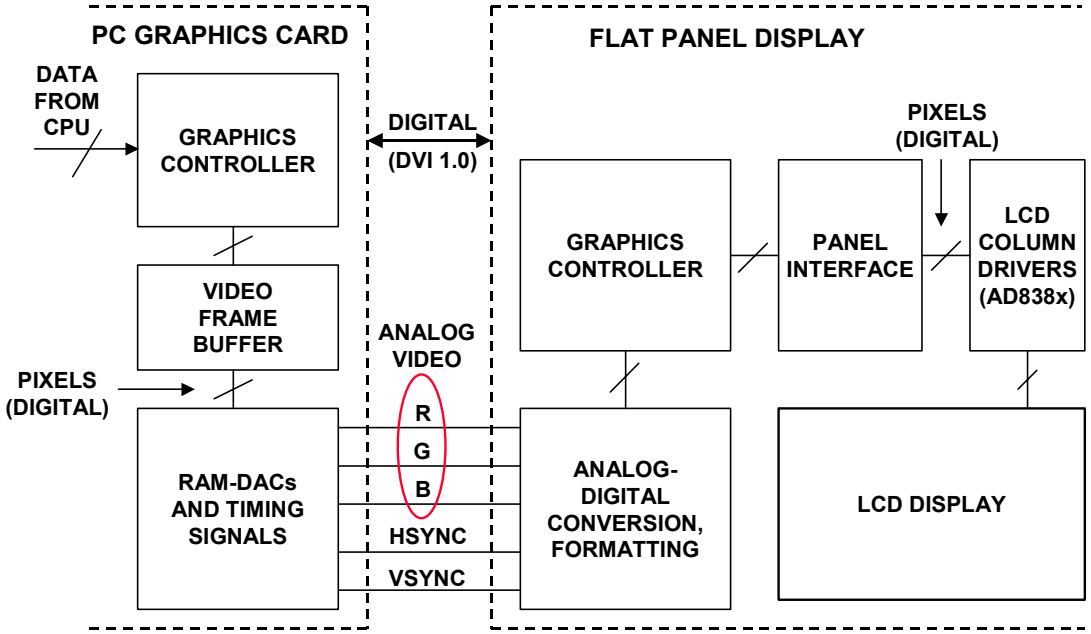


Figure 8.94: *Flat Panel Analog and Digital Interfaces*

For current flat panel displays, ICs such as the AD9888 (Reference 23) digitize the analog RGB data, generate a pixel clock from the HSYNC, and provide other functions necessary to format the pixel data which ultimately drives the columns of LCD display. A functional diagram of the AD9888 is shown in Figure 8.95.

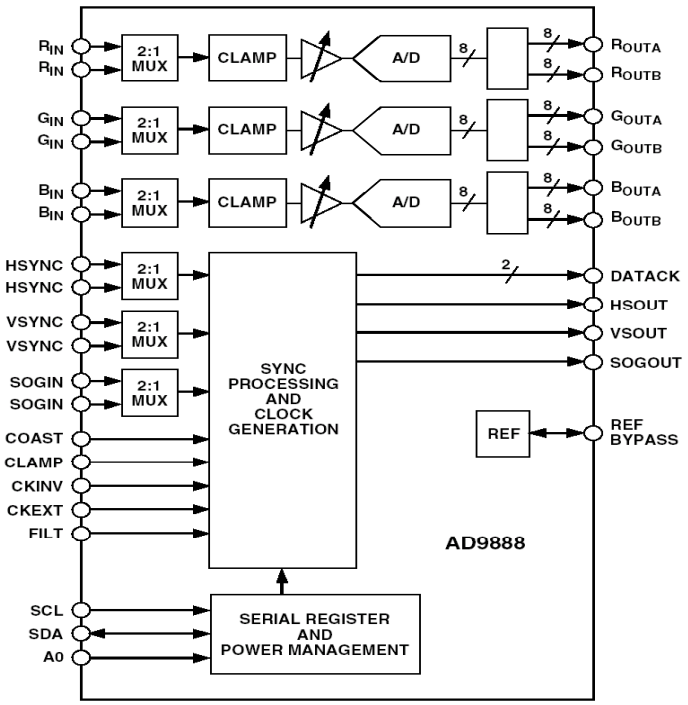


Figure 8.95: *AD9888 100-/140-/170-/205-MSPS Analog Flat Panel Interface*

The AD9888 is a complete 8-bit, 205-MSPS monolithic analog interface optimized for capturing RGB graphics signals from personal computers and workstations. Its 205-MSPS encode rate capability and full-power analog bandwidth of 500 MHz supports resolutions up to UXGA (1600 × 1200 @ 75 Hz). For ease of design and to minimize cost, the AD9888 is a fully integrated interface solution for flat panel displays. The AD9888 includes an analog interface with a 205-MSPS triple ADC with internal 1.25-V reference, PLL to generate a pixel clock from HSYNC and COAST, midscale clamping, and programmable gain, offset, and clamp control. The user provides only a 3.3-V power supply, analog input, and HSYNC and COAST signals. Three-state CMOS outputs may be powered from 2.5 V to 3.3 V.

The AD9888's on-chip PLL generates a pixel clock from HSYNC and COAST inputs. Pixel clock output frequencies range from 10 MHz to 205 MHz. PLL clock jitter is typically less than 450-ps p-p at 205 MSPS. When the COAST signal is presented, the PLL maintains its output frequency in the absence of HSYNC. A sampling phase adjustment is provided. Data, HSYNC, and clock output phase relationships are maintained. The PLL can be disabled and an external clock input can be provided as the pixel clock.

The AD9888 also offers full sync processing for composite sync and sync-on-green applications. A clamp signal is generated internally or may be provided by the user through the CLAMP input pin. This interface is fully programmable via a 2-wire serial interface. Fabricated in an advanced CMOS process, the AD9888 is provided in a space-saving 128-lead MQFP surface-mount plastic package and is specified over the 0°C to 70°C temperature range.

The AD9887A (Reference 24) offers designers the flexibility of an analog interface and digital visual interface (DVI) receiver integrated on a single chip. Also included is support for High Bandwidth Digital Content Protection (HDCP). The AD9887A is a complete 8-bit 170-MSPS monolithic analog interface optimized for capturing RGB graphics signals from personal computers and workstations. Its 170-MSPS sampling rate capability and full-power analog bandwidth of 330 MHz supports resolutions up to UXGA (1600 × 1200 at 60 Hz). The analog interface includes a 170-MHz triple ADC with internal 1.25-V reference, a phase-locked loop (PLL), and programmable gain, offset, and clamp control. The user provides only a 3.3-V power supply, analog input, and HSYNC. Three-state CMOS outputs may be powered from 2.5 V to 3.3 V. The AD9887A's on-chip PLL generates a pixel clock from HSYNC. Pixel clock output frequencies range from 12 MHz to 170 MHz. PLL clock jitter is typically 500-ps p-p at 170 MSPS. The AD9887A also offers full sync processing for composite sync and sync-on-green (SOG) applications. A functional diagram of the AD9887A is shown in Figure 8.96.

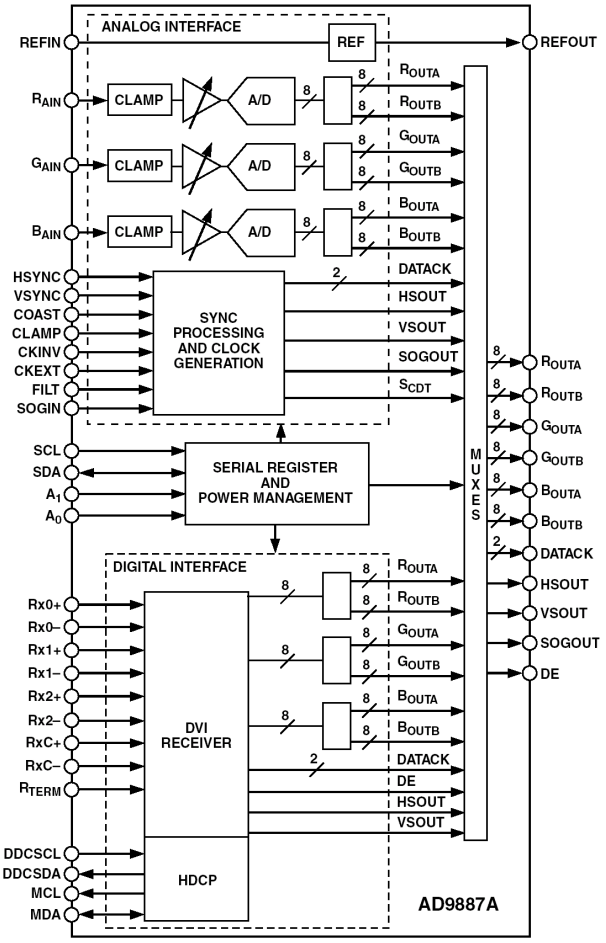


Figure 8.96: *AD9887A Dual Flat Panel Interface*

The AD9887A contains a DVI 1.0 compatible receiver and supports display resolutions up to UXGA (1600 × 1200 at 60 Hz). The receiver operates with true color (24-bit) panels in 1 or 2 pixel(s)/clock mode and features an intra-pair skew tolerance of up to one full clock cycle. With the inclusion of HDCP, displays may now receive encrypted video content. The AD9887A allows for authentication of a video receiver, decryption of encoded data at the receiver, and renewability of that authentication during transmission as specified by the HDCP V1.0 protocol. Fabricated in an advanced CMOS process, the AD9887A is provided in a 160-lead MQFP surface-mount plastic package and is specified over the 0°C to 70°C temperature range.

CCD Imaging Electronics

The *charge-coupled-device* (CCD) and *contact-image-sensor* (CIS) are widely used in consumer imaging systems such as scanners and digital cameras. A generic block diagram of an imaging system is shown in Figure 8.97. The imaging sensor (CCD, CMOS, or CIS) is exposed to the image or picture much like film is exposed in a camera. After exposure, the output of the sensor undergoes some analog signal processing and then is digitized by an ADC. The bulk of the actual image processing is performed using fast digital signal processors. At this point, the image can be manipulated in the digital domain to perform such functions as contrast or color enhancement/correction, etc.

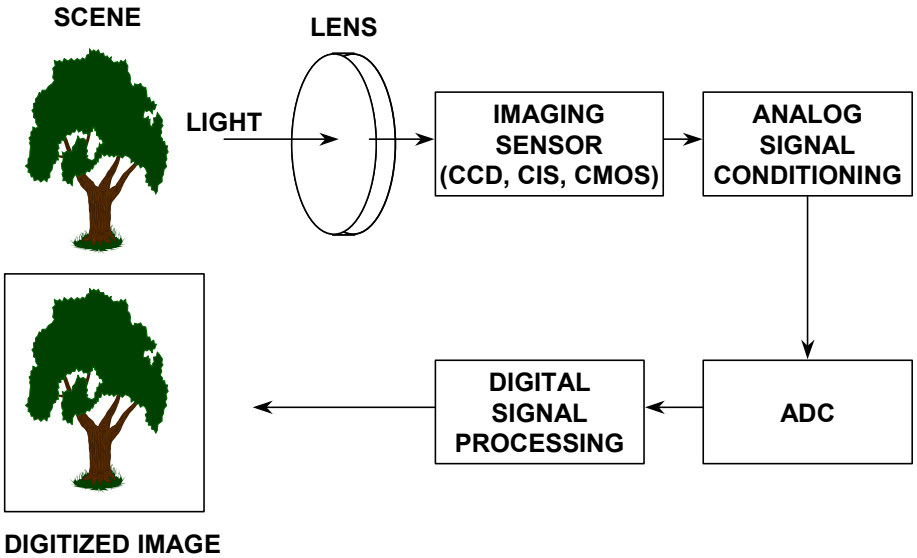


Figure 8.97: *Generic Imaging System for Scanners or Digital Cameras*

The building blocks of a CCD are the individual light sensing elements called pixels (see Figure 8.98). A single pixel consists of a photo sensitive element, such as a photodiode or photocapacitor, which outputs a charge (electrons) proportional to the light (photons) that it is exposed to. The charge is accumulated during the exposure or integration time, and then the charge is transferred to the CCD shift register to be sent to the output of the device. The amount of accumulated charge will depend on the light level, the integration time, and the quantum efficiency of the photo sensitive element. A small amount of

charge will accumulate even without light present; this is called dark signal or dark current and must be compensated for during the signal processing.

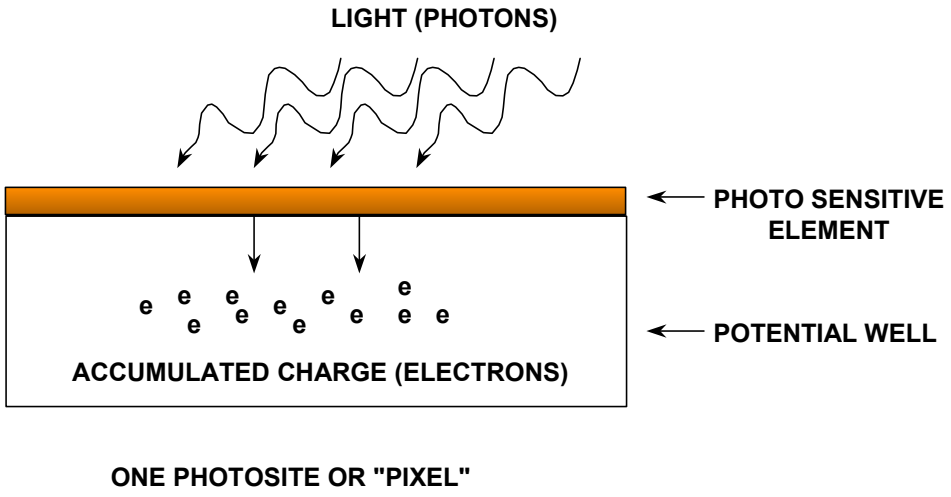


Figure 8.98: *Light Sensing Element*

The pixels can be arranged in a linear or area configuration as shown in Figure 8.99. Clock signals transfer the charge from the pixels into the analog shift registers, and then more clocks are applied to shift the individual pixel charges to the output stage of the CCD. Scanners generally use the linear configuration, while digital cameras use the area configuration. The analog shift register typically operates at pixel frequencies between 1 and 10 MHz for linear sensors, and 5 to 25 MHz for area sensors.

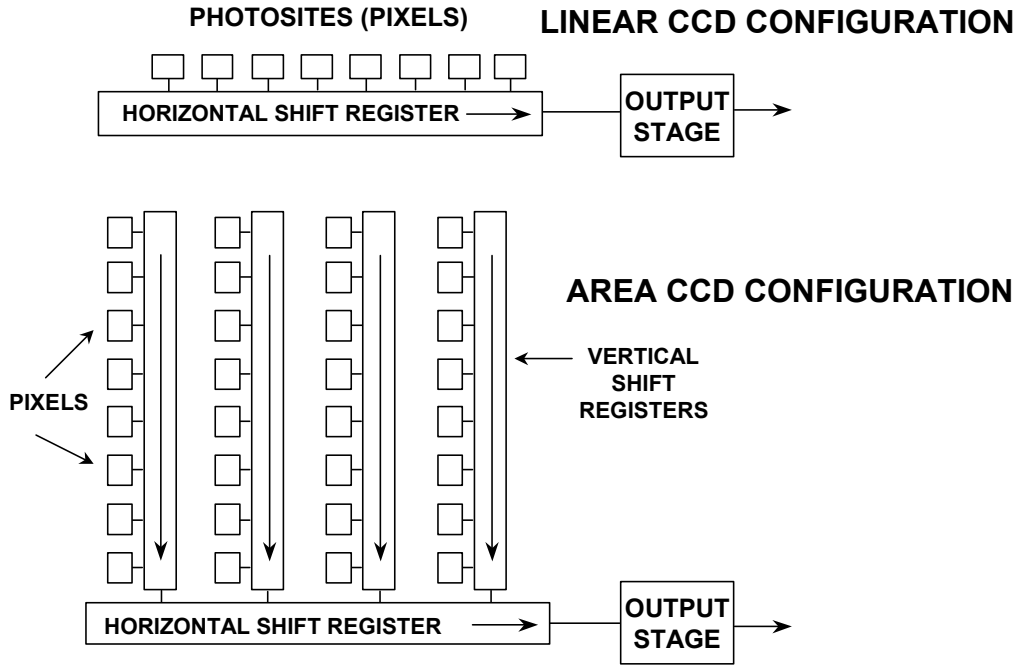


Figure 8.99: *Linear and Area CCD Arrays*

A typical CCD output stage is shown in Figure 8.100 along with the associated voltage waveforms. The output stage of the CCD converts the charge of each pixel to a voltage via the sense capacitor, C_S. At the start of each pixel period, the voltage on C_S is reset to the reference level, V_{REF}, causing a reset glitch to occur. The amount of light sensed by each pixel is measured by the difference between the reference and the video level, ΔV. CCD charges may be as low as 10 electrons, and a typical CCD output has a sensitivity of 0.6 µV/electron. Most CCDs have a saturation output voltage of about 500 mV to 1 V for area sensors and 2 V to 4 V for linear sensors. The dc level of the waveform is between 3 V and 7 V.

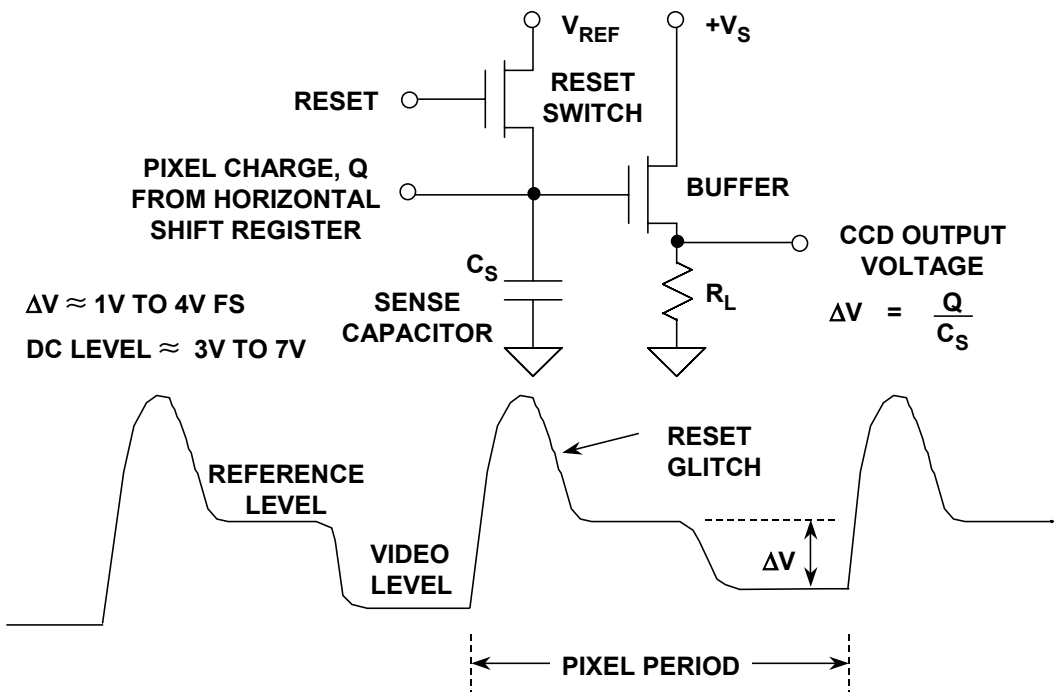


Figure 8.100: *Output Stage and Waveforms*

CCD processes generally have limited capability to perform on-chip signal conditioning. Therefore the CCD output is generally processed by external conditioning circuits. The nature of the CCD output requires that it be clamped before being digitized by the ADC. In addition, offset and gain functions are generally part of the analog signal processing.

CCD output voltages are small and quite often buried in noise. The largest source of noise is the thermal noise in the resistance of the FET reset switch. This noise may have a typical value of 100- to 300-electrons rms (approximately 60- to 180-mV rms). This noise, called "kT/C" noise, is illustrated in Figure 8.101. During the reset interval, the storage capacitor C_S is connected to V_{REF} via a CMOS switch. The on-resistance of the switch (R_{ON}) produces thermal noise given by the well known equation:

$$\text{Thermal Noise} = \sqrt{4kT \cdot BW \cdot R_{ON}}\ . \qquad \text{Eq. 8.14}$$

The noise occurs over a finite bandwidth determined by the R_{ON} C_S time constant. This bandwidth is then converted into equivalent noise bandwidth by multiplying the single-pole bandwidth by $\pi/2$ (1.57):

$$\text{Noise BW} = \frac{\pi}{2}\left[\frac{1}{2\pi R_{ON}C_S}\right] = \frac{1}{4R_{ON}C_S}. \qquad \text{Eq. 8.15}$$

Substituting into the formula for the thermal noise, note that the R_{ON} factor cancels, and the final expression for the thermal noise becomes:

$$\text{Thermal Noise} = \sqrt{\frac{kT}{C}}. \qquad \text{Eq. 8.16}$$

This is somewhat intuitive, because smaller values of R_{ON} decrease the thermal noise but increase the noise bandwidth, so only the capacitor value determines the noise.

Note that when the reset switch opens, the kT/C noise is stored on C_S and remains constant until the next reset interval. It therefore occurs as a *sample-to-sample* variation in the CCD output level and is common to both the reset level and the video level for a given pixel period.

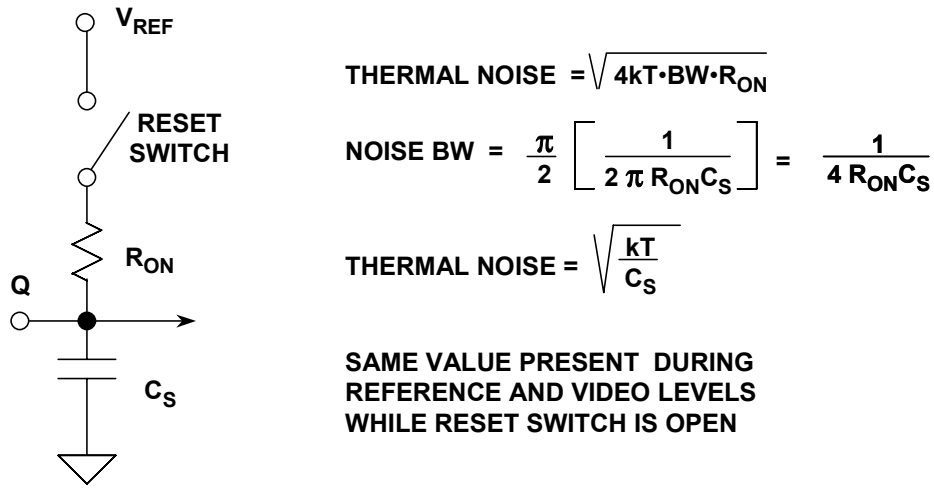


Figure 8.101: *kT/C Noise*

A technique called *correlated double sampling* (CDS) is often used to reduce the effect of this noise. Figure 8.102 shows one circuit implementation of the CDS scheme, though many other implementations exist. The CCD output drives both SHAs. At the end of the reset interval, SHA1 holds the reset voltage level plus the kT/C noise. At the end of the video interval, SHA2 holds the video level plus the kT/C noise. The SHA outputs are applied to a difference amplifier which subtracts one from the other. In this scheme, there is only a short interval during which both SHA outputs are stable, and their difference represents ΔV, so the difference amplifier must settle quickly. Note that the final output is simply the difference between the reference level and the video level, ΔV, and that the kT/C noise is removed.

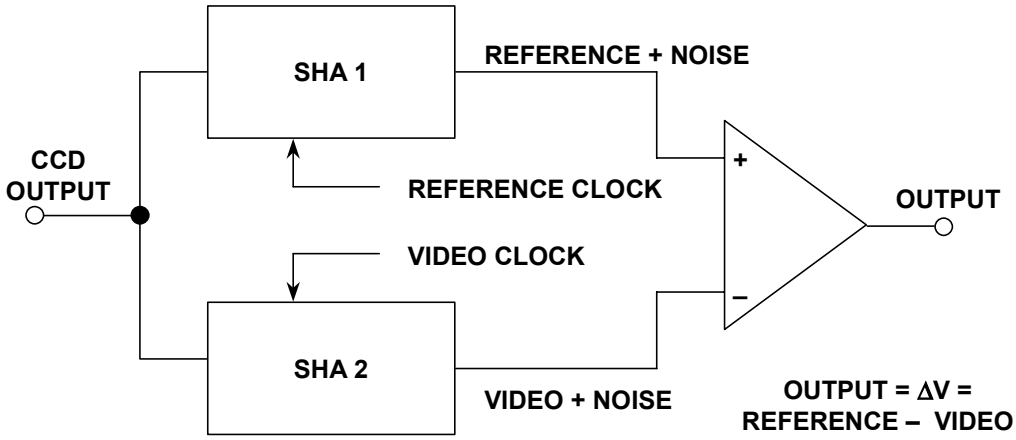


Figure 8.102: *Correlated Double Sampling (CDS)*

Contact Image Sensors (CIS) are linear sensors often used in facsimile machines and low-end document scanners instead of CCDs. Although a CIS does not offer the same potential image quality as a CCD, it does offer lower cost and a more simplified optical path. The output of a CIS is similar to the CCD output except that it is referenced to or near ground (see Figure 8.103), eliminating the need for a clamping function. Furthermore, the CIS output does not contain correlated reset noise within each pixel period, eliminating the need for a CDS function. Typical CIS output voltages range from a few hundred mV to about 1V fullscale. Note that although a clamp and CDS is not required, the CIS waveform must be sampled by a sample-and-hold before digitization.

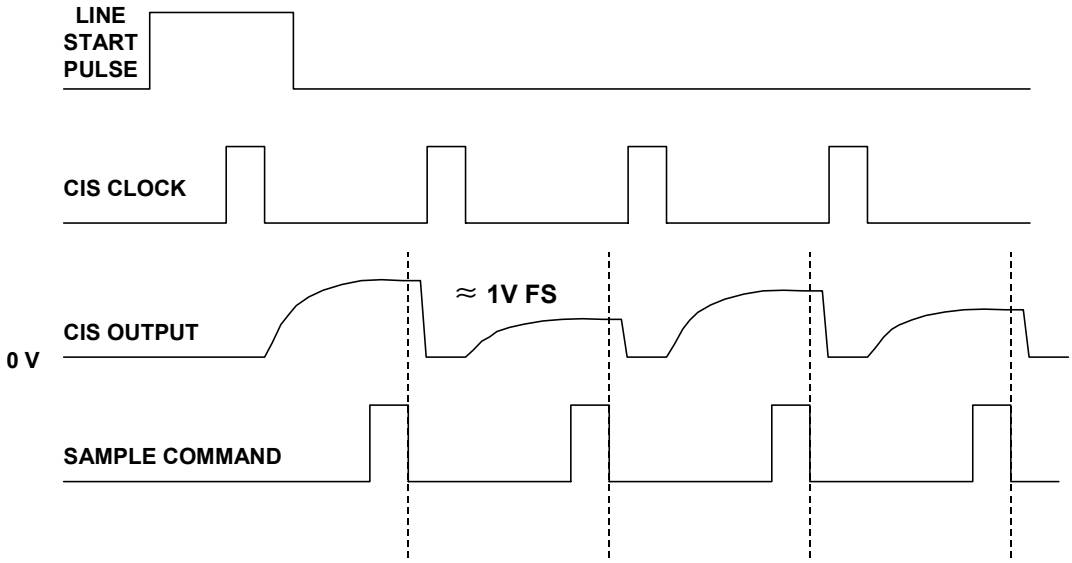


Figure 8.103: *Contact Image Sensor (CIS) Waveforms*

Analog Devices offers several *analog-front-end* (AFE) integrated solutions for the scanner, digital camera, and camcorder markets. They all comprise the signal processing steps described above. Advances in process technology and circuit topologies have made this level of integration possible in foundry CMOS without sacrificing performance. By combining successful ADC architectures with high performance CMOS analog circuitry, it is possible to design complete low cost CCD/CIS signal processing ICs.

The AD9898 (Reference 28) is a highly integrated CCD signal processor for digital still camera and digital video camera applications. A simplified block diagram is shown in Figure 8.104. It includes a complete analog front end with 10-bit A/D conversion combined with a full function programmable timing generator. A precision timing core allows adjustment of high speed clocks with 1-ns resolution at 20-MSPS operation. The AD9898 is specified at pixel rates as high as 20 MHz. The analog front end includes black level clamping, CDS, VGA, and a 10-bit A/D converter. The timing generator provides all the necessary CCD clocks: RG, H-clocks, V-clocks, sensor gate pulses, substrate clock, and substrate bias pulse. Operation is programmed using a 3-wire serial interface. Packaged in a space saving 48-lead LFCSP, the AD9898 is specified over an operating temperature range of –20°C to +85°C.

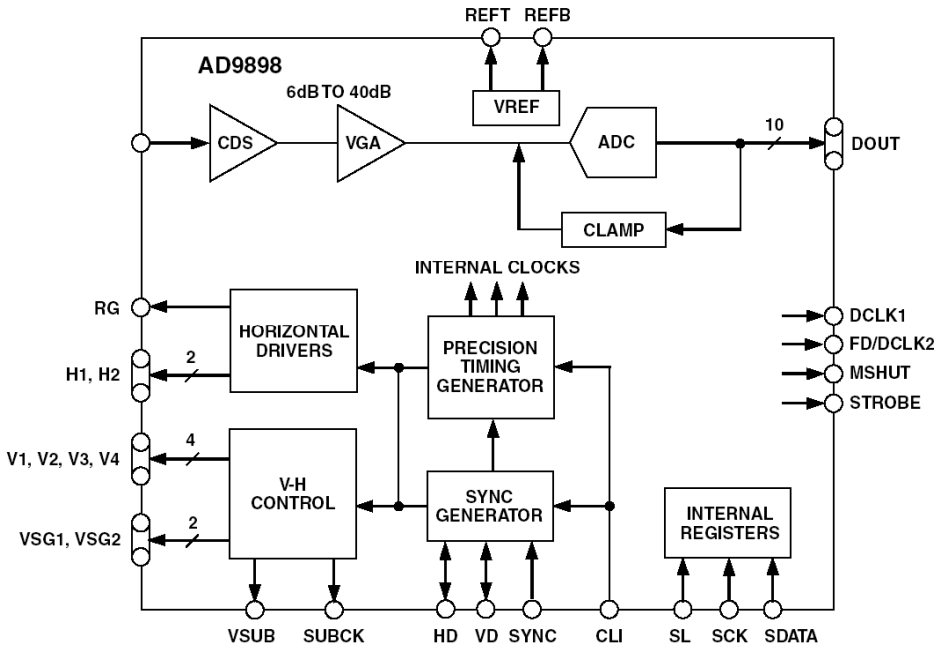


Figure 8.104: *AD9898 CCD Signal Processor with Precision Timing™ Generator*

Three-channel CCD analog front-ends available from Analog Devices include the AD9816 (12-bit), AD9822 (14-bit), AD9814 (14-bit), and the AD9826 (16-bit) processors.

Touchscreen Digitizers

Touchscreens have become widespread in hand held PDAs (Personal Digital Assistants) and other computer products. The majority of PDA makers use a four-wire resistive element as the touchscreen due to its low cost and simplicity. For the touchscreen to interface with the host processor, analog waveforms from the screen must first be converted to digital data (Reference 29, 30).

The user enters data on the screen with a stylus. An ADC converts this analog information to digital data that the host microprocessor uses to determine the stylus's position on the screen. There are a number of inherent problems associated with this application that must be overcome by the ADC.

The touchscreen is usually constructed from two layers of transparent resistive material, in most cases indium tin oxide or other resistive polyester material, with silver ink used for electrodes. The resistance of each layer can vary between vendors, but typically ranges from 100 Ω to 900 Ω. The two layers are placed on top of each other on an insulating layer of glass as shown in Figure 8.105.

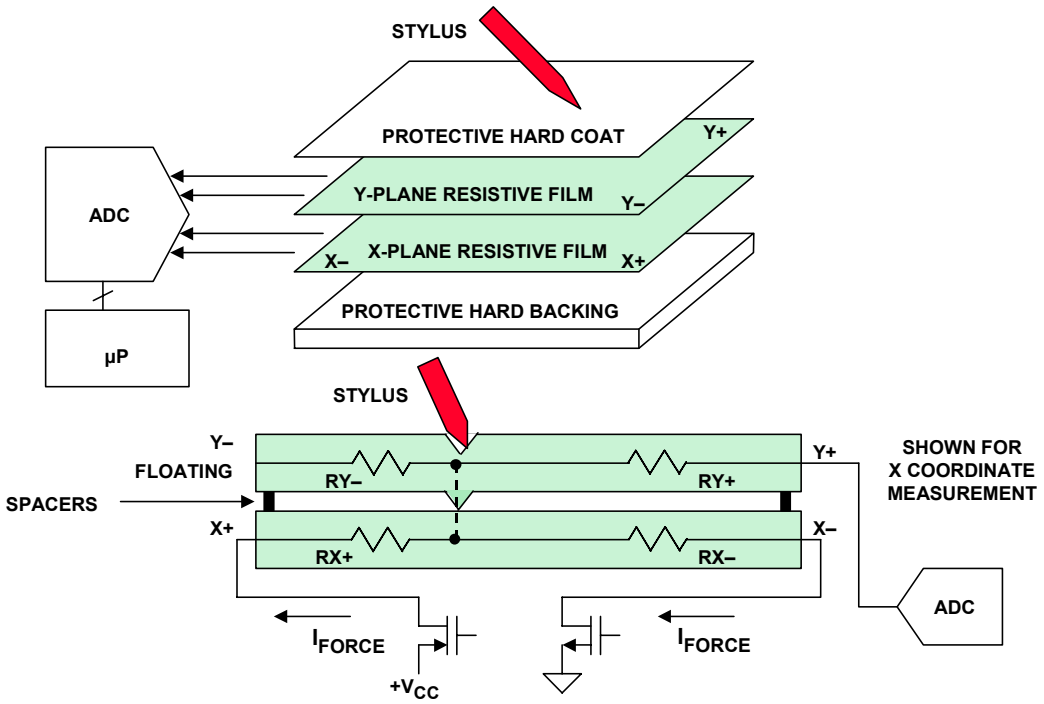


Figure 8.105: *4-Wire Resistive Touchscreen ADC Interface*

During coordinate measurement, one of the resistive planes is powered through on-chip switches on the controller ADC. For X coordinate measurement, the X plane is powered. The Y plane senses where the pen is located on the powered plane. When the pen depresses on the screen, the planes short at this location (shown as the dotted line in the diagram). The voltage detected on the sense plane is proportional to the location of the touch on the powered plane. The Y coordinate can be measured by applying power to the Y plane, using the X plane to sense the position. Thus, X and Y coordinates can be digitized from the screen. The digital code is then operated on by the host CPU, and

character recognition and position information can be achieved. Two methods for making the actual measurements are shown in Figure 8.106.

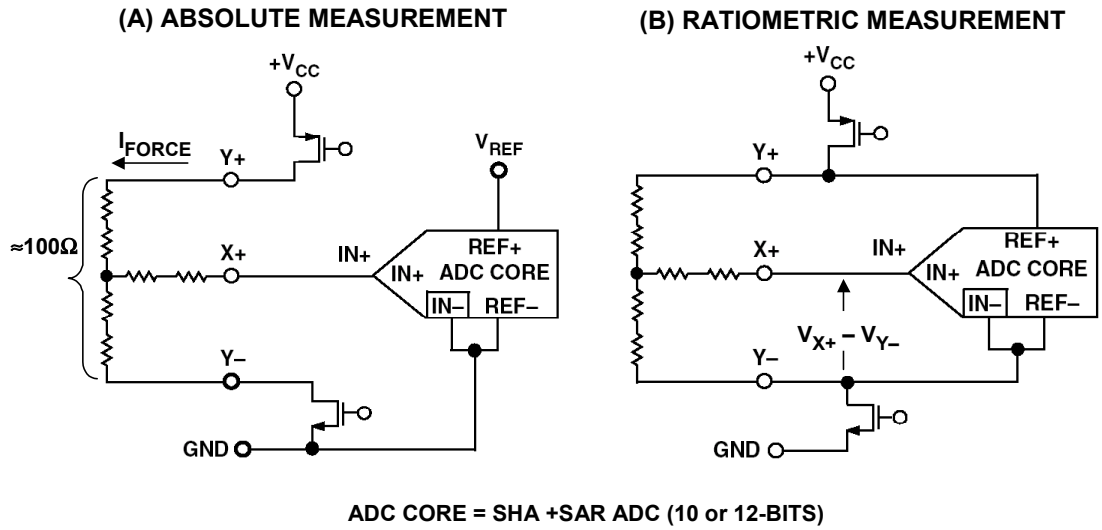


Figure 8.106: *Absolute and Ratiometric Measurements of Touchscreen Voltages*

Figure 8.106A shows a direct, or absolute measuring technique. This method has several problems. Because the impedance of the screen can be 100 Ω or less, the on-chip switches must be carefully designed. For example, assume the system has a 3.3-V supply and a 100-Ω touchscreen. The switches must be capable of sourcing and sinking 33 mA when powering the screen.

The on-chip switches themselves pose another difficulty. They have an inherent ON-resistance, which when powering the screen, results in a voltage drop across the switch. For example, with the 100-Ω screen, if the on-chip switches have ON-resistance values around 10 Ω, then with one switch to the power supply and another to ground, 20% of the ADC's dynamic range is lost. The full supply voltage can never be developed across the screen. In addition, the temperature coefficient of the ON-resistance and the touchscreen resistance can introduce further errors.

Figure 8.106B shows a ratiometric measuring technique which eliminates most of the errors associated with the absolute measurement. In this method, the REF+ and REF– voltages are taken directly across the ends of the touchscreen resistor. The voltage, $V_{X+} - V_{Y-}$, is therefore proportional to the reference voltage, and the digital code is not affected by changes in the switch ON-resistance or the end-to-end touchscreen resistance. The disadvantage of this method is that the touchscreen end-to-end resistance must be powered during the actual conversion interval since it supplies the reference voltage to the ADC. The power can be considerable—33 mA is required to power a 100-Ω touchscreen on a +3.3-V supply, i.e., 109 mW.

The actual time taken to acquire the input can be roughly 25% of the total time taken to acquire a sample (1.5 µs for AD7873) and convert a sample (6 µs for AD7873) by the successive approximation ADC . In effect, the screen need not be powered when the converter is performing the actual analog-to-digital conversion if the absolute technique is used. It only needs to be powered during the SHA acquisition time. However, in the ratiometric method, the screen must be powered throughout the entire conversion process, as it provides the reference voltage for the ADC.

The AD7873 touchscreen digitizer (Reference 31) has a 12-bit successive approximation ADC with a synchronous serial interface and low ON-resistance switches for driving touch screens (Figure 8.107). The AD7873 operates from a single 2.2-V to 5.25-V power supply and features throughput rates greater than 125 kSPS. The AD7873 features direct battery measurement, temperature measurement, and touch-pressure measurement. The AD7873 also has an on-board reference of 2.5 V which can be used for the auxiliary input, battery monitor, and temperature measurement modes. When not in use, the internal reference can be shut down to conserve power. An external reference can also be applied and can be varied from 1 V to V_{CC}, while the analog input range is from 0 V to V_{REF}.

The device includes a shutdown mode that reduces the current consumption to less than 1 µA. The AD7873 features on-board switches. This, coupled with low power and high-speed operation, makes the device ideal for battery-powered systems such as personal digital assistants with resistive touch screens and other portable equipment. The part is available in a 16-lead 0.15" Quarter Size Outline (QSOP) package, a 16-lead Thin Shrink Small Outline (TSSOP) package, and a 16-lead Lead Frame Chip Scale (LFCSP) package.

The analog input to the ADC is provided via an on-chip multiplexer. This analog input may be any one of the X, Y, and Z panel coordinates, battery voltage, or chip temperature. The multiplexer is configured with low-resistance switches that allow an unselected ADC input channel to provide power and an accompanying pin to provide ground for an external device. For some measurements the ON-resistance of the switches may present a source of error. However, with a ratiometric input to the converter this error can be negated as previously described. A typical application circuit is shown in Figure 8.108.

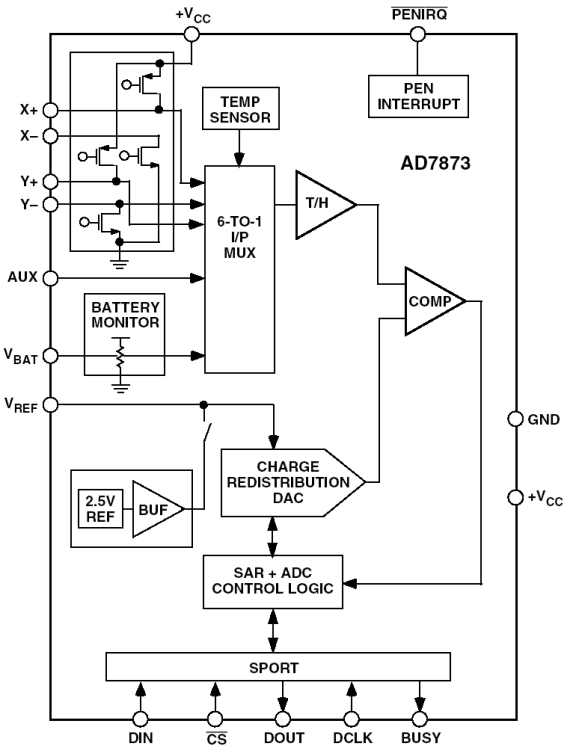


Figure 8.107: *AD7873 Touchscreen Digitizer*

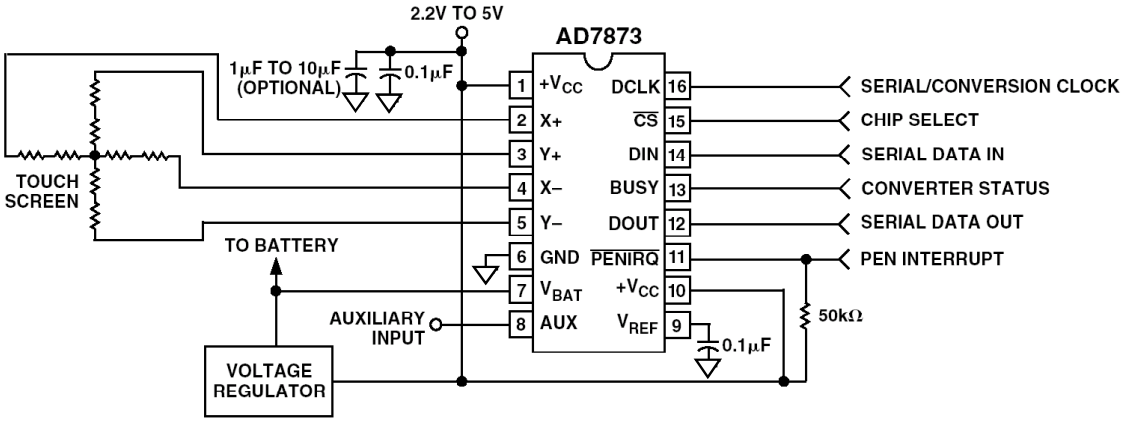


Figure 8.108: *AD7873 Touchscreen Digitizer Application Circuit*

REFERENCES:
8.5 DIGITAL VIDEO AND DISPLAY ELECTRONICS

1. A. Goldberg, "PCM-Encoded NTSC Color Television Subjective Tests," **SMPTE Journal**, Vol. 82, pp. 649-654, Aug. 1973.

2. David E. Acker and Richard H. McLean, "Digital Time-Base Correction for Video Signal Processing," **SMPTE Journal**, Vol. 85, pp. 146-150, March 1976.

3. Walter A. Kester, "Characterizing and Testing A/D and D/A Converters for Color Video Applications," **IEEE Transactions on Circuits and Systems**, Vol. CAS-25, July 1978, pp. 539-550.

4. W. A. Kester, "PCM Signal Codecs for Video Applications," **SMPTE Journal**, Number 88, November 1979, pp. 770-778.

5. W. K. Bucklen, "A Monolithic Video A/D Converter", **Digital Video**, Vol. 2, Society of Motion Picture and Television Engineers, pp. 34-42, March 1979. (Describes the revolutionary TDC1007J. Originally introduced at the 3 Feb. 1979 SMPTE Winter Conference in San Francisco). Bill Bucklen actually accepted an Emmy award in 1988 for this product and was responsible for marketing it to the world).

6. SMPTE 244M, "System M/NTSC Composite Video Signals-Bit Parallel Digital Interface," http://www.smpte.org.

7. IEEE Std. 746-1984, "IEEE Standard for Performance Measurements of A/D and D/A Converters for PCM Television Video Circuits," IEEE, 1984.

8. ITU-Recommendation BT.601, "Universal Sampling Specification for SDTV and HDTV Broadcast Video," http://www.itu.int.

9. SMPTE 125M, "Component Video Signal 4:2:2 Bit-Parallel Digital Interface," http://www.smpte.org.

10. SMPTE 259M, "10-Bit, 4:2:2 Component and $4f_{SC}$ Composite Digital Signals—Serial Digital Interface," http://www.smpte.org.

11. ITU-Recommendation BT.656-4, "Interfaces for Digital Component Video signals in 525-Line and 625-Line Television Systems Operating at the 4:2:2 Level of Recommendation ITU-R BT.601 (Part A)," http://www.itu.int.

12. ITU-Recommendation BT.709-5, "Parameter Values for the HDTV Standards for Production and International Programme Exchange," http://www.itu.int. Also, see SMPTE 296M, SMPTE 274M, http://www.smpte.org.

13. SMPTE 292M, "Bit-Serial Digital Interface for High-Definition Television Systems, http://www.smpte.org.

14. Charles Poynton, **Digital Video and HDTV Algorithms and Interfaces**, Morgan Kaufmann Publishers, 2003, ISBN 1-55860-792-7.

15. Michael Robin and Michel Poulin, **Digital Television Fundamentals**, Second Edition, McGraw-Hill, 2000, ISBN 0-07-135581-2, Chapter 6.

16. Data sheet for ADV7183A 10-Bit NTSC/PAL/SECAM Video Decoder, http://www.analog.com.

17. Data sheet for ADV7310 Multiformat 216 MHz Video Encoder with Six NST™ 12-Bit DACs , http://www.analog.com.

18. Data sheet for ADV7125 CMOS, 330-MHz Triple 8-Bit High Speed Video DAC, http://www.analog.com.

19. Data sheet for ADV7160/ADV7162 96-Bit, 220-MHz True-Color Video RAM-DAC, http://www.analog.com.

20. George Diniz and Tim Stroud, "Bringing Displays into the Digital Future," **EDN**, April 26, 2001, pp. 105-114.

21. Doug Bartow, "Smart Integration in Flat Panel Displays," **Information Display**, Vol. 15, October 1999.

22. Digital Display Working Group, Digital Video Interface Specification, DVI 1.0, http://ddwg.org.

23. Data sheet for AD9888 100/140/170/205MSPS Analog Flat Panel Interface, http://www.analog.com.

24. Data sheet for AD9887A Dual Interface for Flat Panel Displays, http://www.analog.com.

25. Erik Barnes, "High Integration Simplifies Signal Processing for CCDs," **Electronic Design**, February 23, 1998, pp. 81-88.

26. Erik Barnes, "Integrated Front Ends for CCD Signal Processing, **Analog Dialogue,** 32-1, Analog Devices, 1998, http://www.analog.com.

27. Kevin Buckley, "Selecting an Analog Front End for Imaging Applications," **Analog Dialogue**, 34-6, Analog Devices, October, 2000, http://www.analog.com.

28. Data sheet for AD9898 CCD Signal Processor with Precision Timing™ Generator, http://www.analog.com.

29. Paul Kearney, "Configure Your ADC Correctly to Interface with the Display," **Portable Design**, July, 2003.

30. Paul Kearney, "The PDA Challenge-Met by the AD7873 Resistive-Touch-Screen Controller ADC, Analog Dialogue, **Analog Dialogue**, 35-04, Analog Devices, 2001, http://www.analog.com.

31. Data sheet for AD7873 Touchscreen Digitizer, http://www.analog.com

NOTES:

SECTION 8.6: SOFTWARE RADIO AND IF SAMPLING

Walt Kester

Introduction

The term *software radio* had its origins in military intelligence receivers of the late 1980s and the early 1990s (References 1 and 2). Since then, the concept has been widely implemented commercially, especially in cellular radio applications (References 3-18).

A software radio receiver uses an ADC to digitize the analog signal in the receiver as close to the antenna as practical, generally at an intermediate frequency (IF). Hence the term, *IF sampling* came into being. Once digitized, the signals are filtered, demodulated, and separated into individual channels using specialized DSPs called *receive signal processors* (RSPs). Similarly, a software radio transmitter performs coding, modulation, etc., in the digital domain—and near the final output IF stage, a DAC is used to convert the signal back to an analog format for transmission. The DSP which precedes the DAC is referred to as the transmit signal processor (TSP). A very simplified generic software radio receiver and transmitter are shown in Figure 8.109.

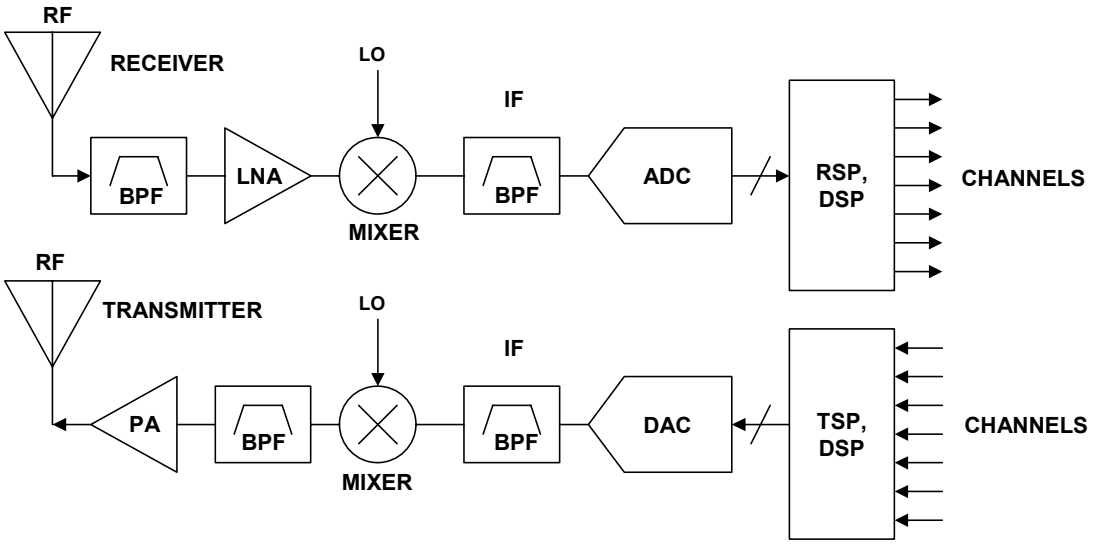


Figure 8.109: *Generic IF Sampling Software Radio Receiver and Transmitter*

Ideally, the software radio eliminates quite a bit of expensive analog signal processing circuitry and performs these functions in low-cost DSPs. The software radio also allows the same hardware to handle various wireless air standards by making changes to the various DSP programs.

Wideband IF sampling places high demands on the ADCs and DACs in terms of SNR and SFDR, as has previously been discussed in Chapter 2. However, converter technology has progressed to the point that software radio is practical for most of the

popular wireless air standards. For high volume applications, such as cellular telephone basestations and handsets, software radio has become a reality and a necessity.

Evolution of Software Radio

In order to understand the evolution of software radio, consider the analog superheterodyne receiver invented in 1917 by Major Edwin H. Armstrong (see Figure 8.110). This architecture represented a significant improvement over single-stage direct conversion (homodyne) receivers which had previously been constructed using tuned RF amplifiers, a single detector, and an audio gain stage. A significant advantage of the superhetrodyne receiver is that it is much easier and more economical to have the gain and selectivity of a receiver at fixed intermediate frequencies (IF) than to have the gain and frequency-selective circuits "tune" over a band of frequencies.

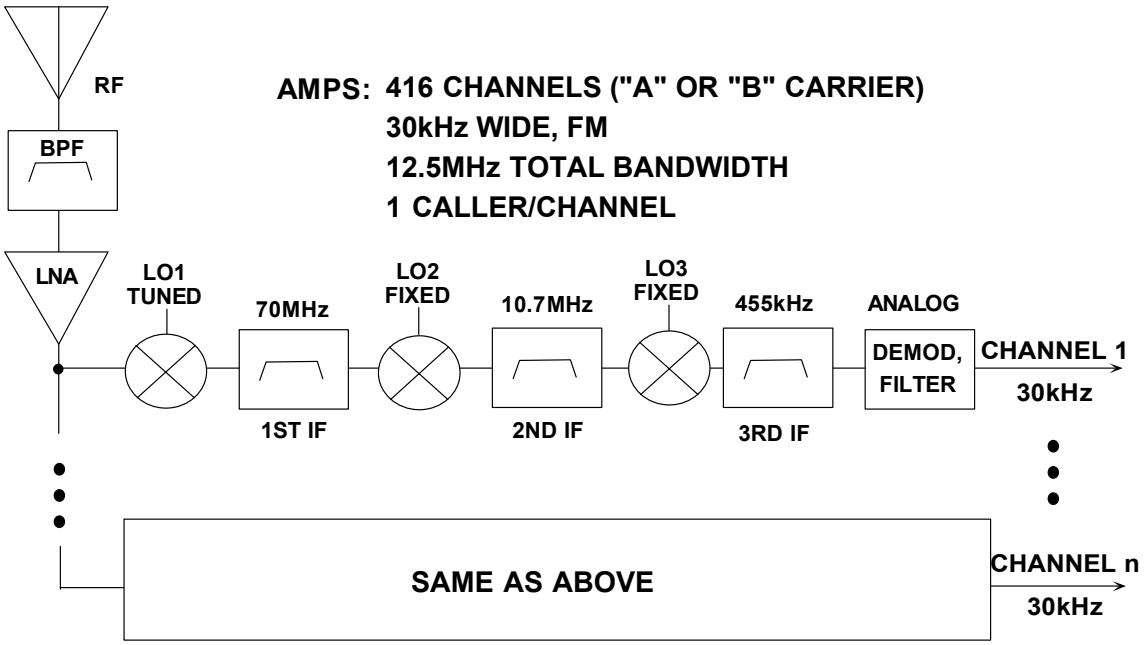


Figure 8.110: *U.S. Advanced Mobile Phone Service (AMPS) Superheterodyne Analog Receiver*

The frequencies shown in Figure 8.110 correspond to the AMPS (Advanced Mobile Phone Service) analog cellular phone system currently used in the U.S., but quickly being phased out in favor of other digital standards. The receiver is designed for AMPS signals at 900-MHz RF. The signal bandwidth for the "A" or "B" carriers serving a particular geographical area is 12.5 MHz (416 channels, each 30kHz wide). The receiver shown uses triple conversion, with a first IF frequency of 70 MHz and a second IF of 10.7 MHz, and a third IF of 455 kHz. The image frequency at the receiver input is separated from the RF carrier frequency by an amount equal to twice the first IF frequency (illustrating the point that using relatively high first IF frequencies makes the design of the image rejection filter easier).

The output of the third IF stage is demodulated using analog techniques (discriminators, envelope detectors, synchronous detectors, etc.). In the case of AMPS, the modulation is

FM. An important point to notice about the above scheme is that there is *one receiver required per channel*, and only the antenna, prefilter, and LNA can be shared.

It should be noted that in order to make the receiver diagrams more manageable, the interstage amplifiers are not shown. They are, however, an important part of the receiver, and the reader should be aware that they must be present.

Receiver design is a complicated art, and there are many tradeoffs that can be made between IF frequencies, single-conversion vs. double-conversion or triple conversion, filter cost and complexity at each stage in the receiver, demodulation schemes, etc. There are many excellent references on the subject, and the purpose of this section is only to acquaint the design engineer with some of the emerging architectures, especially in the application of ADCs and DACs in the design of advanced communications receivers.

A Receiver Using Digital Processing at Baseband

With the availability of high performance high speed ADCs and DSPs, it is now becoming common practice to use digital techniques in at least part of the receive and transmit path, and various chipsets are available from Analog Devices to perform these functions for GSM and the other cellular standards. This is illustrated in Figure 8.111, where the output of the last IF stage is converted into a baseband in-phase (I) and quadrature (Q) signal using a quadrature demodulator. The I and Q signals are then digitized by a dual ADC. The RSPs/DSPs then perform the additional signal processing. The signal can then be converted into analog format using a DAC, or it can be processed, mixed with other signals, upconverted, and retransmitted.

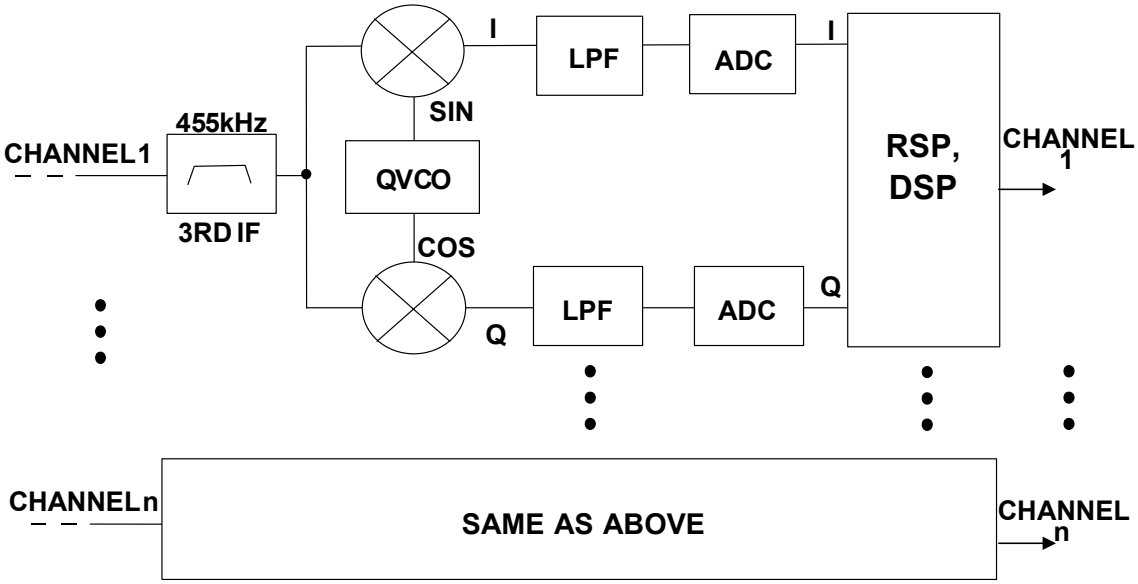


Figure 8.111: *Digital Receiver Using Baseband Sampling and Digital Processing*

At this point, we should make it clear that *a digital receiver is not the same thing as digital modulation*. In fact, a digital receiver will do an excellent job of receiving an analog signal such as AM or FM. Digital receivers can be used to receive any type of modulation standard including analog (AM, FM) or digital (QPSK, QAM, FSK, GMSK, etc.). Furthermore, since the core of a digital radio is its digital signal processor (RSP/DSP), the same receiver can be used for both analog and digitally modulated signals (simultaneously if necessary), assuming that the RF and IF hardware in front of the RSP/DSP is properly designed. Since it is software that determines the characteristics of the radio, changing the software changes the radio. For this reason, digital receivers are often referred to as *software radios*.

The fact that a radio is software programmable offers many benefits. A radio manufacturer can design a generic radio in hardware. As air interface standards change (as from AMPS to IS-136, or IS-95), the manufacturer is able to make timely design changes to the radio by reprogramming the RSP/TSP/DSP. From a user or service-provider's point of view, the software radio can be upgraded by loading the new software at a small cost, while retaining all of the initial hardware investment. Additionally, the receiver can be tailored for custom applications at very low cost, since only software costs are involved.

A digital receiver performs the same function as an analog one with one difference; some of the analog functions have been replaced with their digital equivalent. The main difference between Figure 8.110 and Figure 8.111 is that the FM discriminator in the analog radio has been replaced with two ADCs and a RSP/DSP. While this is a very simple example, it shows the fundamental beginnings of a digital, or *software* radio.

An added benefit of using digital techniques is that some of the filtering in the radio is now performed digitally. This eliminates the requirement of tight tolerances and matching for frequency-sensitive components such as inductors and capacitors. In addition, since filtering is performed within the RSP/ DSP, the filter characteristics can be implemented in software instead of costly and sensitive SAW, ceramic, or crystal filters. In fact, many filters can be synthesized digitally that could never be implemented in a strictly analog receiver.

This simple example is only the beginning. With current technology, much more of the receiver and transmitter can be implemented in digital form. There are numerous advantages to moving the digital portion of the radio closer to the antenna. In fact, placing the ADC at the output of the RF section and performing direct RF sampling might seem attractive, but does have some serious drawbacks, particularly in terms of selectivity and out-of-band (image) rejection. However, the concept makes clear one key advantage of software radios: they are programmable and require little or no component selection or adjustments to attain the required receiver performance.

Narrowband IF-Sampling Digital Receivers

A reasonable compromise in many digital receivers is to convert the signal to digital form at the output of the first or the second IF stage. This allows for out-of-band signals to be filtered before reaching the ADC. It also allows for some automatic gain control (AGC) in the analog stage ahead of the ADC to reduce the possibility of in-band signals

overdriving the ADC and allows for maximum signal gain prior to the A/D conversion. This relieves some of the dynamic range requirements on the ADC. Additionally, IF sampling and digital receiver technology reduce costs by elimination of further IF stages (mixers, filters, and amplifiers) and adds flexibility by the replacement of fixed analog filter components with programmable digital ones.

In analyzing an analog receiver design, much of the signal gain is after the first IF stage. This prevents front-end overdrive due to out-of-band signals or strong in-band signals. However, in an IF sampling digital receiver, all of the gain is in the front end, and great care must be taken to prevent in-band and out-of-band signals from saturating the ADC, which results in excessive distortion. Therefore, a method of attenuation must be provided when large in-band signals occur. While additional signal gain can be obtained digitally after the ADC, there are certain restrictions. Gain provided in the analog domain improves the SNR of the signal and only reduces the performance to the degree that the noise figure (NF) degrades noise performance.

Figure 8.112 shows a detailed IF sampling digital receiver for the GSM/EDGE (900 MHz) system. The receiver has RF gain, automatic gain control (AGC), a high performance ADC, digital receive signal processor (RSP), and a DSP.

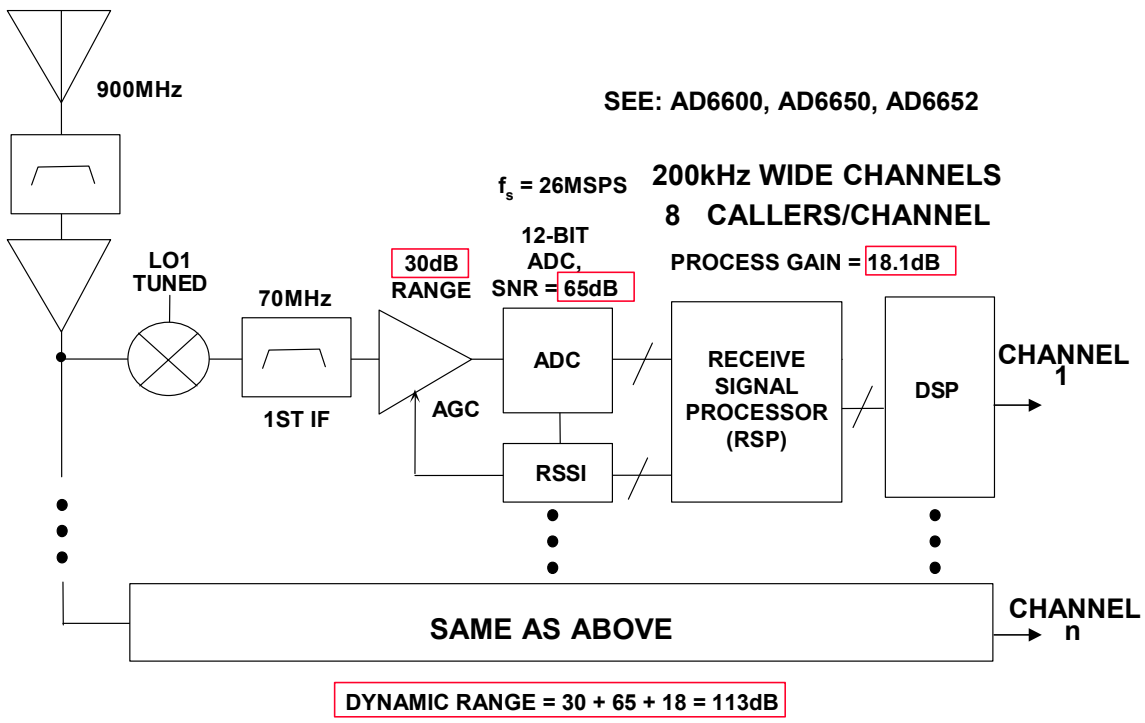


Figure 8.112: *Narrowband IF Sampling GSM/EDGE Digital Receiver*

The heart of the system is the 12-bit 26-MSPS ADC with AGC, the RSSI (Received Signal Strength Indicator), and the RSP. Various chipsets are available which perform these functions for GSM/EDGE (see AD6600, AD6650, AD6620, AD6624, and AD6634) and for WCDMA (see AD6634, and AD6652).

GSM/EDGE (Europe) and IS-136 (United States) are similar multicarrier time-division-multiplexed-access (TDMA) systems, while IS-95, IS-95B, WCDMA, and CDMA2000 are spread spectrum code-division-multiple-access systems (CDMA). The channel bandwidth for CDMA systems is either 1.25 MHz for IS-95, IS-95B, and CDMA2000, or 5 MHz for WCDMA. There will be more details on these air standards later in this section.

The GSM/EDGE 900-MHz air standard is one of the most stringent with respect to ADC dynamic range, and therefore a narrowband receiver design is most often implemented. In the system shown in Figure 8.112, the total dynamic range is 113 dB comprised by the AGC loop (30 dB), ADC SNR (65 dB), and the process gain (18.1 dB).

The bandwidth of a single GSM channel is 200 kHz, and each channel can handle up to 8 simultaneous callers. A typical basestation may be required to handle 50 to 60 simultaneous callers, thereby requiring 8 separate signal processing channels.

Figure 8.113 shows the IF frequency of 71.5 MHz centered in the 6th Nyquist zone sampled at a frequency of 26 MSPS. The RSP reverses the frequency sense of the signal when it is translated to the first Nyquist zone as shown.

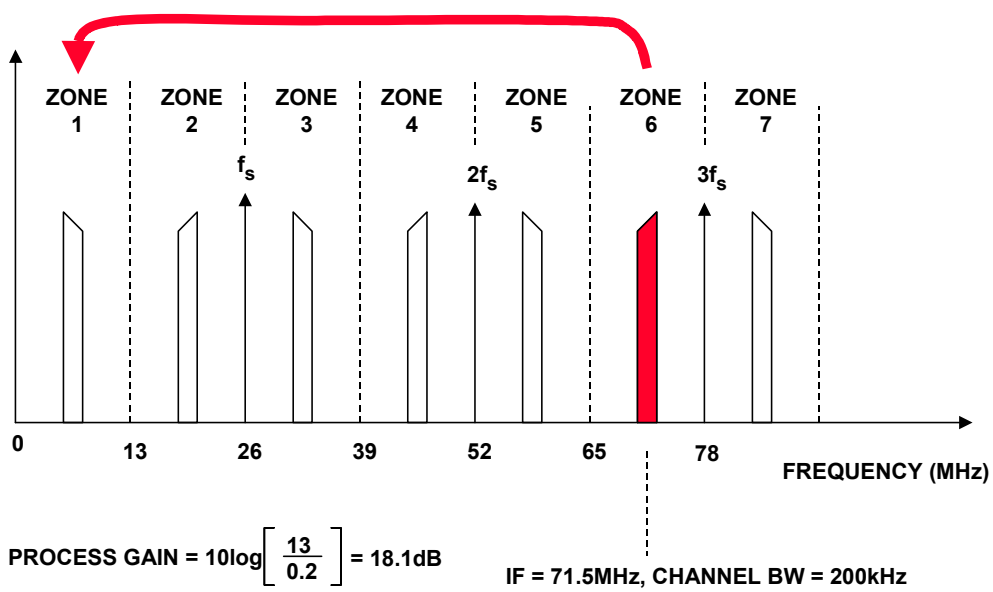


Figure 8.113: *Narrowband GSM Receiver Bandpass Sampling of a 200-kHz Channel at 26 MSPS*

We now have a 200-kHz baseband signal (generated by undersampling) which is being sampled at 26 MSPS as shown in Figure 8.114A. The RSP then translates the signal to baseband as shown in Figure 8.114B.

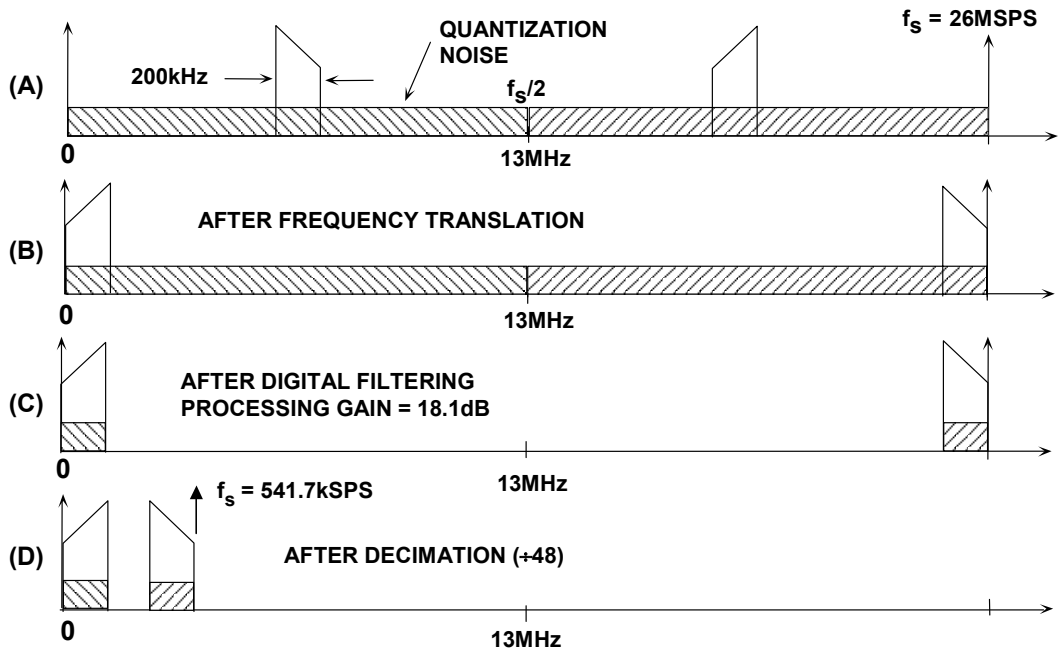


Figure 8.114: *Digital Filtering and Decimation of the 200kHz GSM Channel*

The signal is then passed through a digital filter in the RSP which removes all frequency components above 200 kHz, including the quantization noise which falls in the region between 200 kHz and 13 MHz (the Nyquist frequency) as shown in Figure 8.114C. The resultant increase in SNR is 18.1 dB (processing gain). There is no information contained in the signal above 200 kHz, and the output data rate can be reduced (decimated) from 26 MSPS to 541.7 kSPS, a data rate which the DSP can handle, as shown in Figure 8.114D. The data corresponding to the 200-kHz channel is transmitted to the DSP over a simple 3-wire serial interface. The DSP then performs such functions as channel equalization, decoding, and spectral shaping.

The concept of *processing gain* is common to all communications systems, analog or digital, and was discussed in Chapter 2 of this book. In a sampling system, the quantization noise produced by the ADC is spread over the entire Nyquist bandwidth which extends from dc to $f_S/2$. If the signal bandwidth, BW, is less than $f_S/2$, digital filtering can remove the noise components outside this bandwidth, thereby increasing the effective SNR. The processing gain in a sampling system can be calculated from the formula:

$$\text{Processing Gain} = 10\log\left(\frac{f_S}{2\cdot \text{BW}}\right). \qquad \text{Eq. 8.17}$$

The SNR (noise measured over $f_S/2$ bandwidth) of the ADC at the bandwidth of the signal should be used to compute the actual narrowband SNR by adding the processing gain determined by the above equation. If the ADC is an ideal N-bit converter, then its SNR (measured over the Nyquist bandwidth) is 6.02N + 1.76 dB.

Notice that as shown in the previous narrowband receiver example, there can be processing gain even if the original signal is an undersampled one. The only requirement is that the signal bandwidth be less than $f_S/2$, and that the noise outside the signal bandwidth be removed with a digital filter.

Wideband IF-Sampling Digital Receivers

Thus far, we have avoided a detailed discussion of *narrowband* versus *wideband* digital receivers. A digital receiver can be either, but more detailed definitions are important at this point. By *narrowband*, we mean that sufficient pre-filtering has been done such that all undesired signals have been eliminated and that only the signal of interest is presented to the ADC input. This is the case for the GSM/EDGE basestation example previously discussed.

Wideband simply means that a number of channels are presented to the input of the ADC, and further filtering, tuning, and processing is performed digitally. Usually, a wideband receiver is designed to receive an entire band of cellular or other similar wireless services. In fact, one wideband digital receiver can be used to receive *all* channels within the band simultaneously, allowing almost all of the analog hardware (including the ADC) to be shared among all channels as shown in Figure 8.115, which compares the narrowband and the wideband approaches.

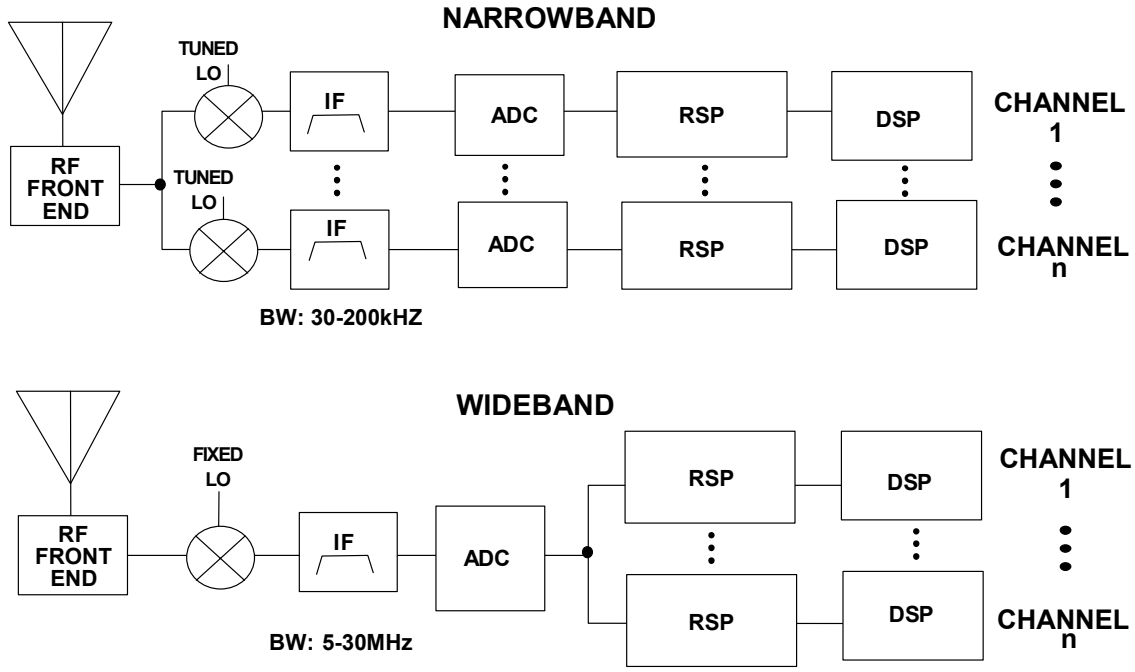


Figure 8.115: *Narrowband Versus Wideband Digital Receiver*

Note that in the narrowband digital radio, there is one front-end LO and mixer required per channel to provide individual channel tuning. In the wideband digital radio, however, the first LO frequency is fixed, and the "tuning" is done in the RSP circuits following the ADC.

A typical wideband digital receiver may process a 5-MHz to 30-MHz band of signals simultaneously. This approach is frequently called *block conversion*. In the wideband digital receiver, the variable local oscillator in the narrowband receiver has been replaced with a fixed oscillator, so tuning must be accomplished digitally. Tuning is performed using a digital down converter (DDC) and digital filter called a *channelizer*. The term channelizer is used because the purpose of these chips is to select one channel out of the many within the broadband spectrum actually present in the ADC output. A typical RSP is shown in Figure 8.116.

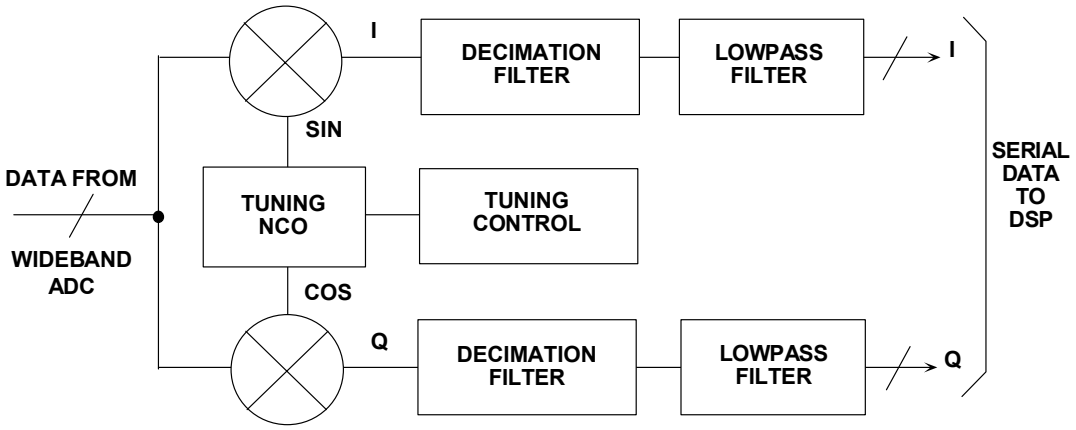


Figure 8.116: *Receive Signal Processing (RSP) in Wideband Receiver (Simplified)*

It consists of an NCO (Numerically Controlled Oscillator) with tuning capability, dual mixer, and matched digital filters. These are the same functions that would be required in an analog receiver, but implemented in digital form. The digital output from the channelizer is the demodulated signal in I and Q format, and all other signals have been filtered and removed. Since the channelizer output consists of one selected RF channel, one channelizer is required for each channel. The channelizer also serves to decimate the output data rate such that it can be processed by a DSP. The DSP extracts the signal information from the I and Q data and performs further processing. Another effect of the filtering provided by the channelizer is to increase the SNR by adding processing gain as previously described.

The design of a complete wideband receiver is a major project and is highly dependent on the particular air standard. Figure 8.117 shows the approximate evolution of the wireless air standards starting with the first generation (1G) analog systems, progressing to the various TDMA/FDM (time-division-multiple-access, frequency-division-multiplex) and the CDMA (code-division-multiple-access) digital systems of the second-generation (2G), followed by an intermediate generation referred to as 2.5G, and through the projected 3G standards of the future. Details of this evolution can be found in Reference 16.

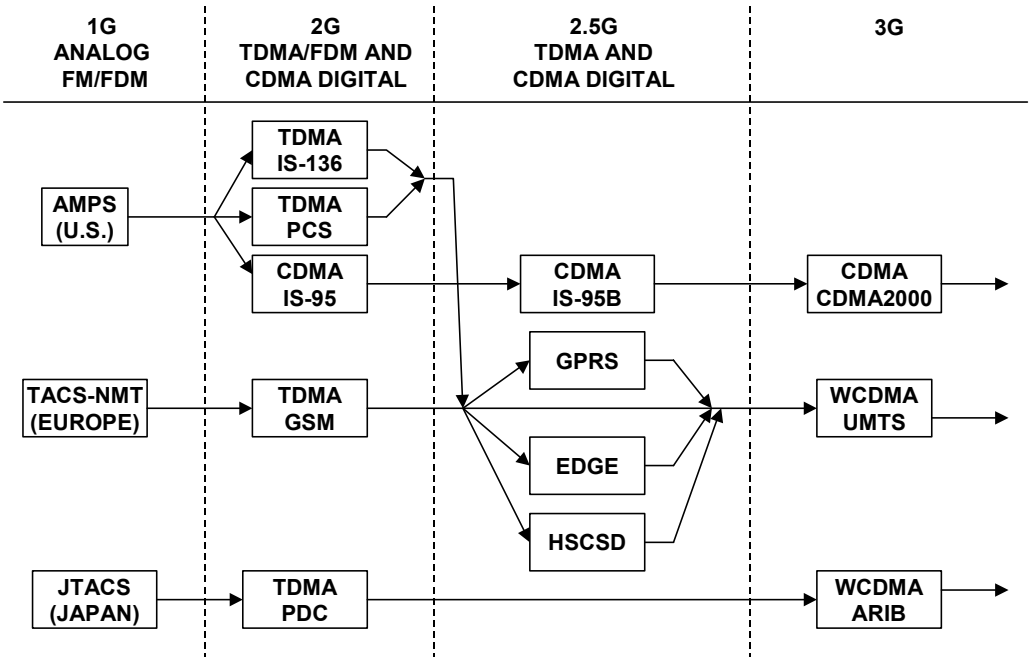


Figure 8.117: *1st Generation to 3rd Generation Wireless Evolution*

From a spectral standpoint, there are basically two types of digital air standards. The TDMA/FDM standards use various time slots to multiplex the data on the different channels, and the resulting carriers are then multiplexed in frequency (FDM), with a spacing between channels of either 30 kHz or 200 kHz depending upon the air standard. The total bandwidth allocation per provider for these systems can range from 5 MHz to 15 MHz.

The second class of standards are the ones which use code-division-multiple-access (CDMA) techniques, sometimes referred to as *spread-spectrum*. In these systems, a pseudo-random number sequence modulates the channel data frequency, and the receiver uses an identical sequence to recover the channel data. The combination of multiple channels appears approximately as random noise spread over a bandwidth of either 1.25 MHz or 5 MHz depending on the air standard. Bandwidth allocations per provider of 5 MHz to 20 MHz are typical for these systems.

The wireless spectrum is very crowded and contains many large signals which cause "blockers" from one band to interfere with desired signals in another. Regardless of the air standard, there are many signals which can interfere with the desired carriers. Figure 8.118 shows a typical RF spectrum where numerous narrowband signals surround the two CDMA2000 carriers located midband. The receiver must tolerate all of the narrowband signals while still maintaining the required sensitivity as defined by the particular air standard.

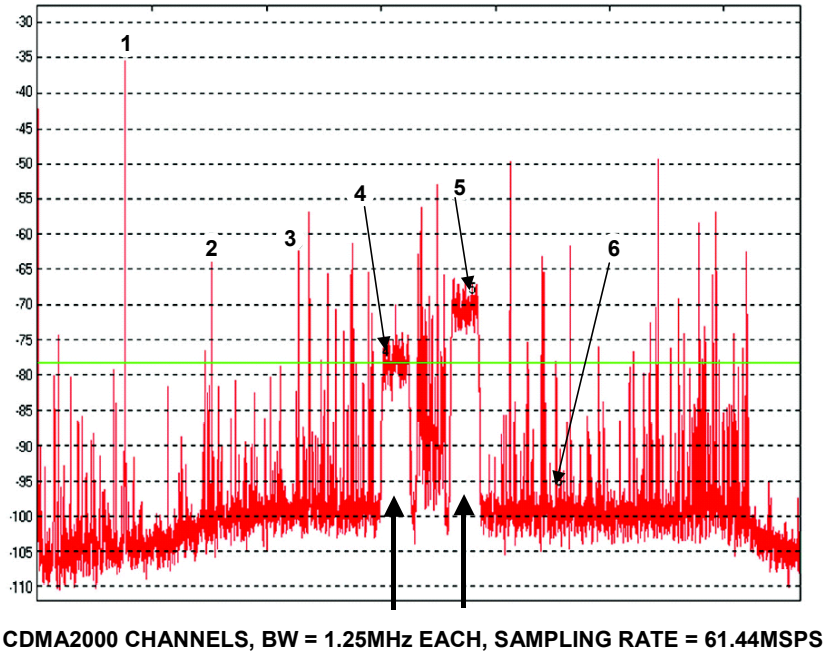


Figure 8.118: *Typical RF Spectrum of a Multicarrier CDMA2000 Receiver*

We begin our brief look at receivers for various air standards with the AMPS analog system which is ideally suited to the wideband digital receiver design. A simplified diagram of a suitable wideband digital receiver is shown in Figure 8.119. The AD6645 sampling frequency of 61.44 MSPS is chosen to be a power-of-two multiple of the channel bandwidth (30 kHz × 2024 = 61.44 MSPS). The choice of IF frequency is flexible, and a second IF stage may be required if lower IF frequencies are chosen.

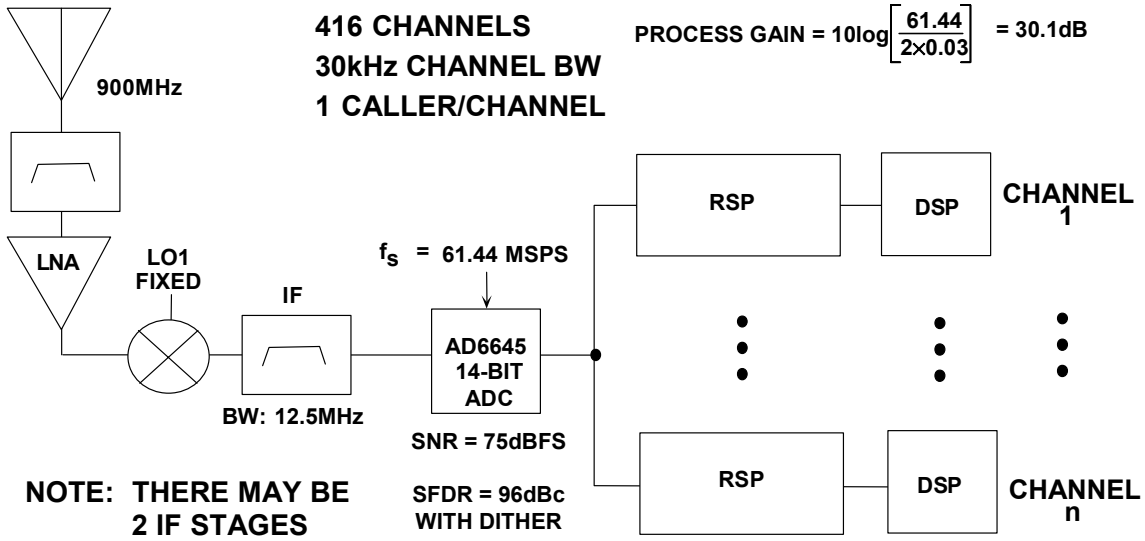


Figure 8.119: *AMPS Wideband Digital Receiver*

With a sampling frequency of 61.44 MSPS, the 12.5-MHz bandwidth signal can be positioned in the first Nyquist zone (dc to 30.72 MHz) with an IF frequency of 15.36 MHz, or in the second Nyquist zone (30.72 MHz to 61.44 MHz) with an IF frequency of 46.08 MHz.

The receive signal processors (RSPs) provide the receiver tuning and demodulate the signal into the I and Q components. The output data rate to the DSPs after decimation is approximately 60 kSPS. The processing gain incurred for a sampling frequency of 61.44 MSPS is calculated as follows:

$$\text{Processing Gain} = 10\log\left(\frac{61.44}{2\times 0.03}\right) = 30.1\,\text{dB}. \qquad \text{Eq. 8.18}$$

The SNR of the AD6645 over the Nyquist bandwidth is 75 dB, and when the process gain of 30.1 dB is added, the SNR in the 30-kHz bandwidth is 75 + 30.1 = 105.1 dB. The SFDR of the AD6645 is greater than 96 dBc for signals several dB below fullscale (with dither added). The following analysis shows that these values are more than adequate to meet the minimum AMPS requirements for sensitivity of –116 dBm with a blocker level of –26 dBm.

The simplified AMPS receiver analysis for spurious requirements begins as shown in Figure 8.120.

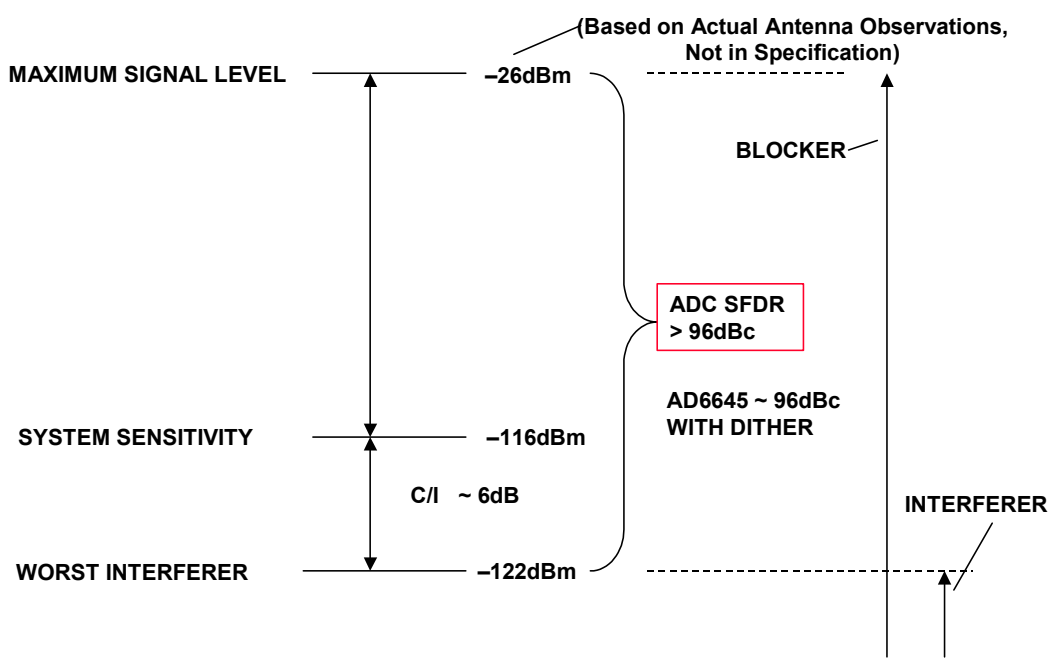


Figure 8.120: *AMPS Spurious Requirements*

The maximum blocker level is –26 dBm (there is no actual specification for this—it was determined by actual measurements at Analog Devices). The minimum detectable signal (sensitivity) is specified as –116 dBm. Approximately 6-dB carrier-to-interferer ratio (C/I) is required to prevent the interferer from overtaking the desired signal. Therefore, for an input signal of –26 dBm, the worst allowable spurious signal must be at –122 dBm. This implies a minimum SFDR requirement of –26 dBm –(–122 dBm) = 96 dBc. The AD6645 14-bit ADC will meet this requirement with dither added (see discussion on dither later in this section) for a signal 5-dB below the ADC fullscale input of +5 dBm. In practice, dither is not generally used because there is additional margin in the design because the blocker level of –26 dBm (measured, not specified) is a very conservative number, and in practice can be reduced by several dB without affecting overall system performance.

The simplified AMPS receiver requirement for sensitivity (relating to ADC SNR) is shown in Figure 8.121.

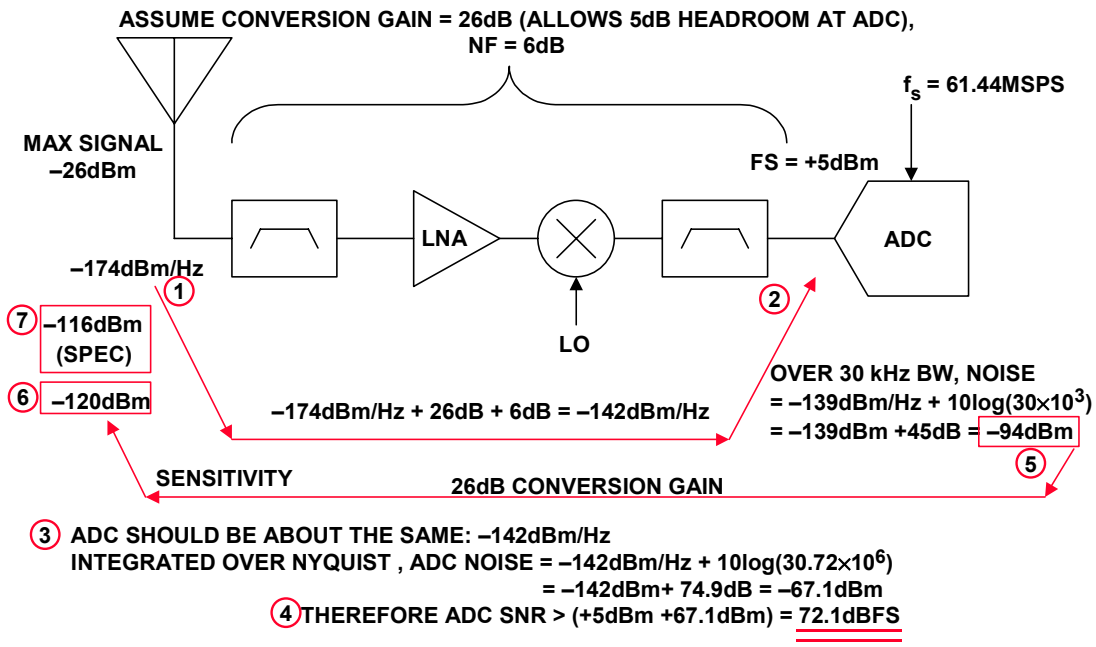


Figure 8.121: *AMPS Receiver Sensitivity Requirements*

The fullscale input of the ADC is +5 dBm (2.2-V p-p into 200 Ω, matched to 50 Ω with a 1:4 impedance-ratio RF transformer). Allowing 5-dB headroom at the ADC input, this requires a gain from the antenna to the ADC (conversion gain) of 26 dB, which causes the –26-dBm signal at the antenna to appear as a 0-dBm signal at the ADC input. Assume an overall noise figure (NF) of 6 dB for the receiver, which represents a good design. The thermal noise at the antenna input is –174 dBm/Hz (see Chapter 2). The noise reflected to the ADC input is therefore

$$\text{ADC Input Noise} = -174\text{dBm/Hz} + 26\text{ dB (Conversion Gain)} + 6\text{ dB (NF)} = -142\text{ dBm/Hz.} \qquad \text{Eq. 8.19}$$

Now, assume that the input noise due to the ADC is approximately the same, and this places the total noise at the ADC input at –139 dBm/Hz (degraded by 3 dB).

When integrated over the 30-kHz channel bandwidth, this noise becomes:

$$\text{Noise in 30-kHz channel} = -139\ \text{dBm/Hz} + 10\log(30\times10^3) = -139\text{dBm} + 45\ \text{dB} = -94\ \text{dBm}. \quad \text{Eq. 8.20}$$

When reflected back to the antenna by the conversion gain of 26 dB, this yields a sensitivity of –94 dBm – 26 dB = –120 dBm. This is 4-dB better than the required sensitivity of –116 dBm.

This assumes the ADC can meet the –142-dBm/Hz noise specification. This noise must be integrated over the Nyquist bandwidth (30.72 MHz) to obtain the data sheet number.

$$\text{ADC Noise}_{\text{Nyquist}} = -142\ \text{dBm/Hz} + 10\log(30.72\times10^6) = -142\ \text{dBm} + 74.9\ \text{dB} = -67.1\ \text{dBm}. \quad \text{Eq. 8.21}$$

Since the fullscale ADC input is +5 dBm, the minimum SNR requirement for the ADC is

$$\text{ADC SNR}_{\text{Nyquist}} = +5\ \text{dBm} - (-67.1\ \text{dBm}) = 72.1\ \text{dBFS}. \quad \text{Eq. 8.22}$$

The SNR specification for the AD6645 is 75 dBFS for a 15-MHz input signal, and it therefore meets the sensitivity requirement with nearly 3-dB margin.

The various steps in this analysis are numbered inside the circles in Figure 8.121 to make them easier to follow.

Needless to say, there are a number of other ways to approach this receiver design analysis, and many tradeoffs can be made between the various parameters, but the simple method and numbers used above serve to illustrate the process, especially as it relates to the approximate ADC requirements.

Figure 8.122 shows the system requirements for the GSM-900MHz system. This is the most strenuous standard, especially from the standpoint of the ADC. A similar analysis can be used to determine the approximate ADC SFDR requirement. In this case, a C/I ratio of 15 dB is required. The resulting SFDR requirement of 106 dBc cannot be met with current ADCs, therefore narrowband receivers are most often used in this application.

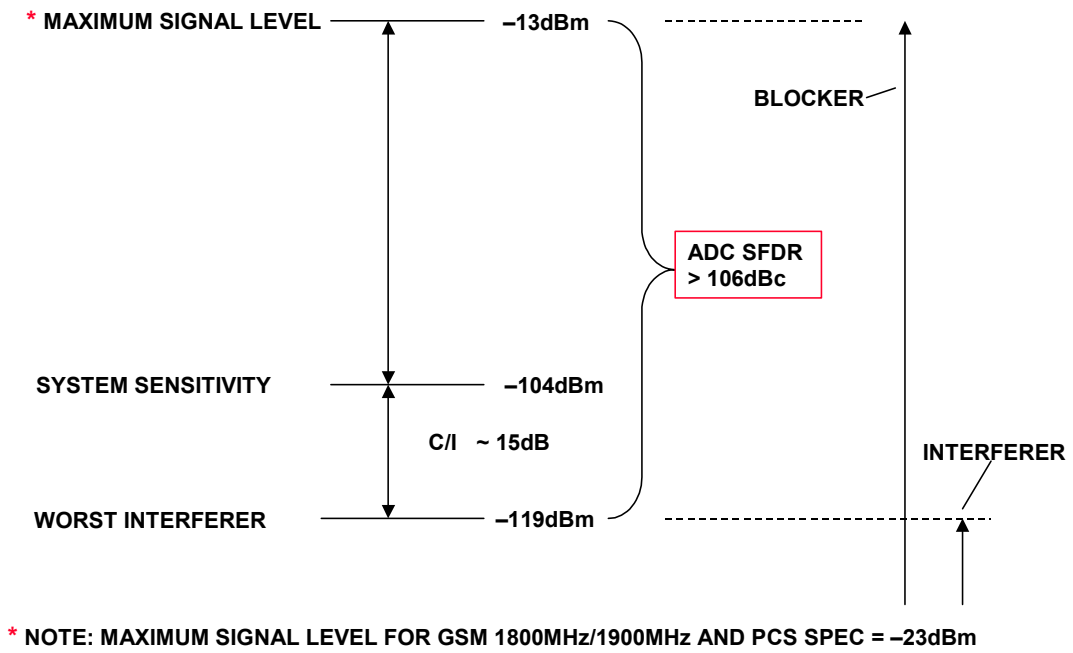


Figure 8.122: *GSM 900-MHz Spurious Requirements*

Figure 8.123 shows the sensitivity analysis for the GSM 900 MHz system. The analysis proceeds along the same lines as in the previous AMPS sensitivity analysis, and the resulting ADC SNR requirement is approximately 85 dBFS which cannot be met with current ADCs—a narrowband approach must therefore be used.

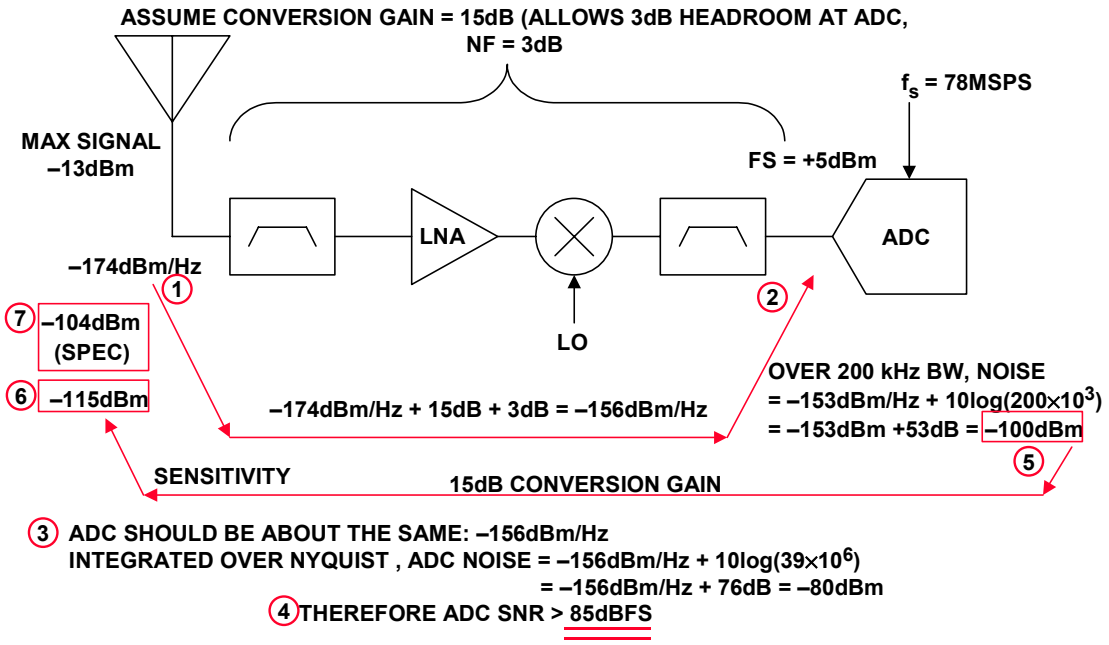


Figure 8.123: *GSM 900 MHz Sensitivity Requirements (ADC SNR)*

Because of the stringent ADC requirements for wideband GSM 900 MHz, the current receivers for this system are typically single-carrier narrowband types as previously discussed (see Figure 8.112 - Figure 8.114).

It should be noted, however, that the GSM-1800MHz/1900MHz (as well as PCS in the U.S.) maximum signal level requirement is reduced to –23 dBm, rather than –13 dBm (the sensitivity requirement is still –104 dBm), and a similar analysis shows an SFDR requirement of 93 dBc and an SNR of 75 dB which are obtainable with modern ADCs such as the AD6645.

In addition to single-tone SFDR, two-tone and multi-tone intermodulation distortion is important in an ADC for wideband receiver applications. Figure 8.124 shows two strong signals in two adjacent channels at frequencies f_1 and f_2. If the ADC has third-order intermodulation distortion, these products will fall at $2f_2 - f_1$ and $2f_1 - f_2$ and are indistinguishable from signals which might be present in these channels. This is one reason the GSM 900-MHz system is difficult to implement using the wideband approach, since the dynamic range requirement is greater than 100 dBc.

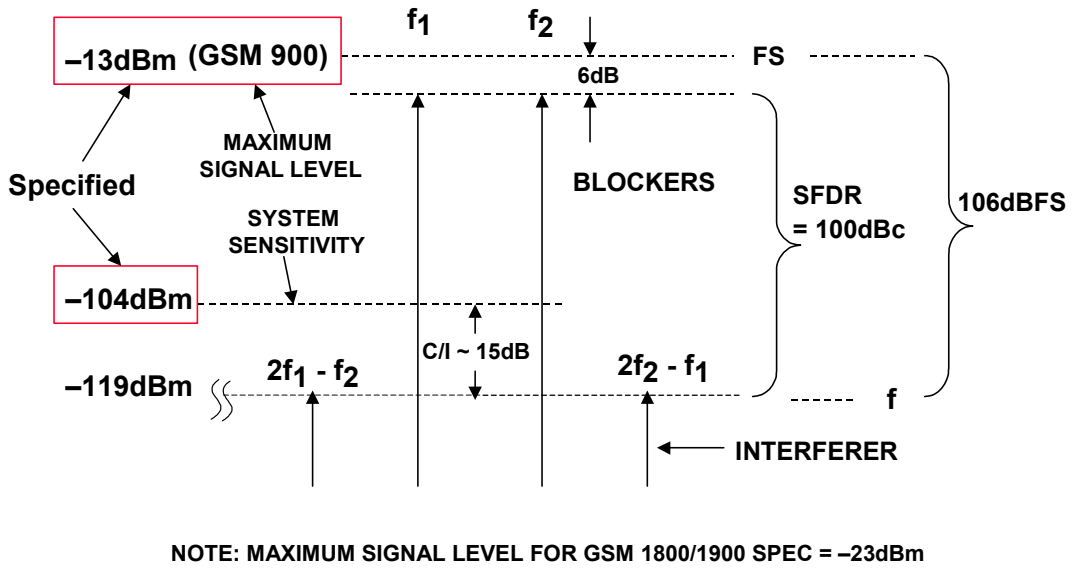


Figure 8.124: *Two-Tone Intermodulation Distortion in Multichannel System (GSM 900-MHz Requirements Shown)*

The two-tone SFDR of the AD6645 is greater than 103 dBFS with input tones at 55.25 MHz and 56.25 MHz as shown in Figure 8.125. The tones are undersampled, so they appear in the Nyquist bandwidth at 80 MHz – 55.25 MHz = 24.75 MHz and at 80 MHz – 56.25 MHz = 23.75 MHz. Note than the amplitude of each tone must be 6-dB below full scale in order to prevent the ADC from being overdriven. It should be noted however that the actual GSM two-tone IMD specification is given for tone levels of –43 dBm. However, this specification was written with single-carrier systems in mind, so the test with tone levels 6-dB below fullscale is more representative of the requirements in a wideband system.

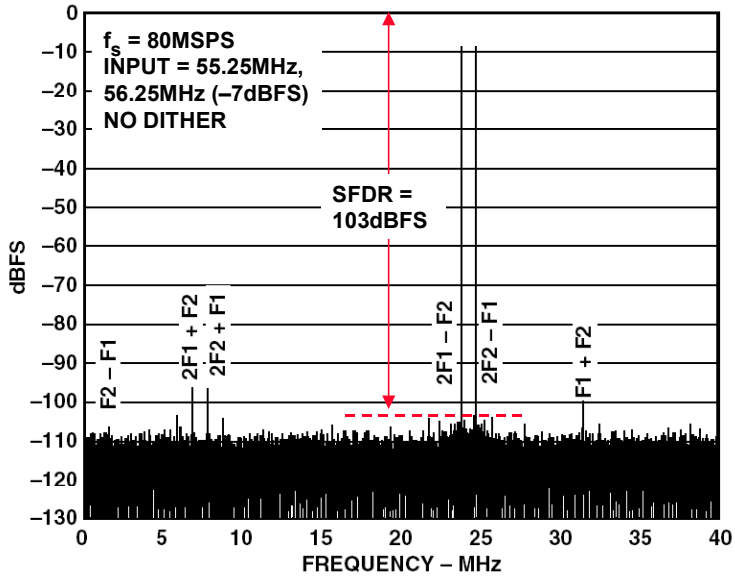


Figure 8.125: *AD6645 Two-Tone Intermodulation Performance*

The requirements for multicarrier CDMA system performance are slightly different from TDMA/FDM systems because of the different architecture. In a CDMA receiver, the information to be transmitted is combined with a pseudorandom number (PN) spreading sequence that has a much wider bandwidth, using a function similar to a mixer. This has the effect of spreading the desired information over the wider bandwidth of the spreading signal as shown in Figure 8.126A and B.

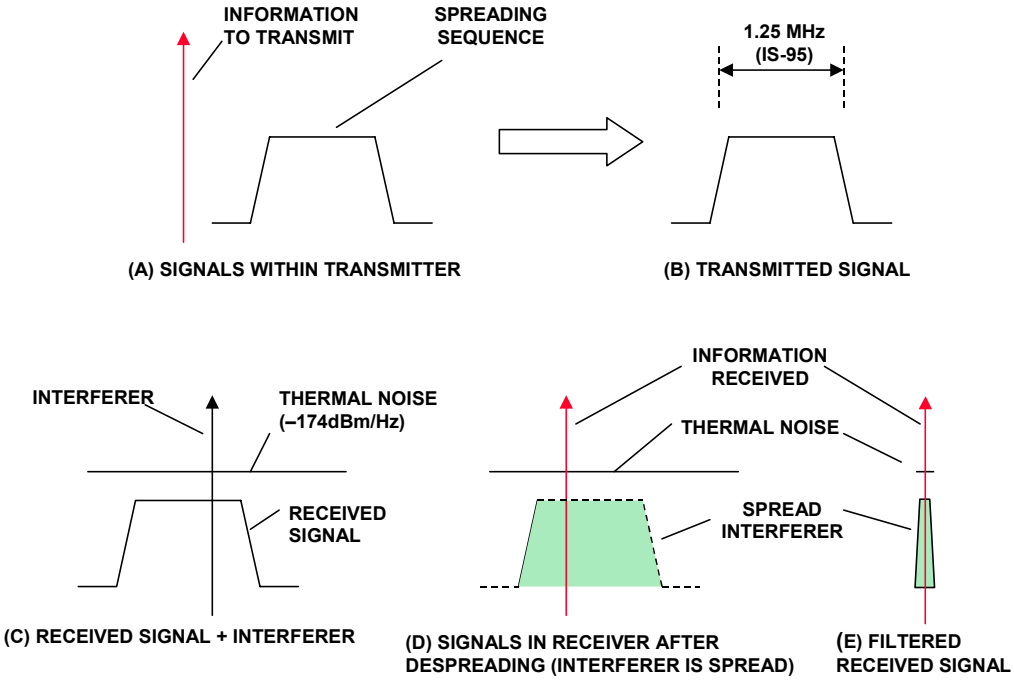


Figure 8.126: *Signals Within a CDMA System*

In the receiver, the same PN sequence is correlated with the incoming signal. The correlation process has the effect of "gathering" the energy of the desired transmission into the original information bandwidth, allowing it to be detected and further processed. At the same time, any energy, including interferers that do not correlate to the PN sequence, become spread over the wider bandwidth of the PN sequence as shown in Figure 8.126C and D.

Since the information bandwidth is now much narrower than the interfering energy, a low pass filter can be used to remove all of the interfering energy, except the small amount that appears in the information bandwidth. This energy typically appears as Gaussian noise.

Figures 8.126D and E show the two components to the noise. The thermal noise present in the receiver is one component. The source of this is available atmospheric noise plus the active noise of the receiver and transmitter. In addition to this is the band limited noise generated by spreading the interferer while the main signal is being despread. Since the receiver does not care about the source of the noise, the effective noise is the root-sum-square of these two.

This information can be used to determine the performance requirements for a 3G receiver, or any other receiver used for spread spectrum reception. Unlike GSM and other narrowband standards, spurious effects usually are not directly specified when it comes to "co-channel" interference, but they may be determined by carefully studying the operations in conjunction with the given standard specifications.

From this it is possible to determine the required performance from an ADC and the rest of the signal chain (a detailed analysis of the requirements for an IS-95 CDMA system can be found in Reference 18).

A digitized undersampled FFT output for a 4-carrier WCDMA system is shown in Figure 8.127. The channel spacing is 5 MHz, and the total bandwidth required for the 4 carriers is approximately 20 MHz. The AD6645 operates at a sampling frequency of 61.44 MSPS. The WCDMA carriers are shifted from a center frequency of 46.08 MHz (2nd Nyquist zone) to the baseband center frequency of 15.36 MHz by the process of undersampling.

Figure 8.128 illustrates an entire 25-MHz bandwith multicarrier signal centered at an IF frequency of 48.75 MHz digitized at 65 MSPS. The AD6645 digitizes signals in the second Nyquist zone with nearly the same dynamic performance as would be obtained if the signal were in the first Nyquist zone.

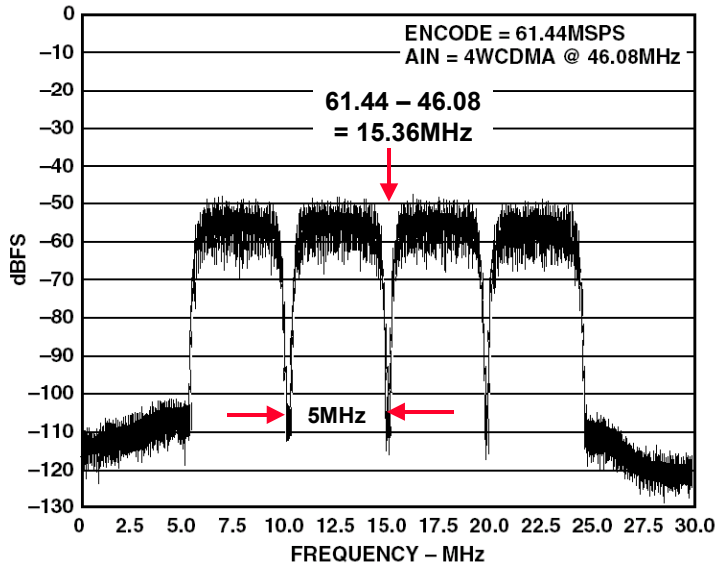


Figure 8.127: *AD6645 Sampling at 61.44 MSPS with 4 WCDMA Inputs Centered at 46.08 MHz*

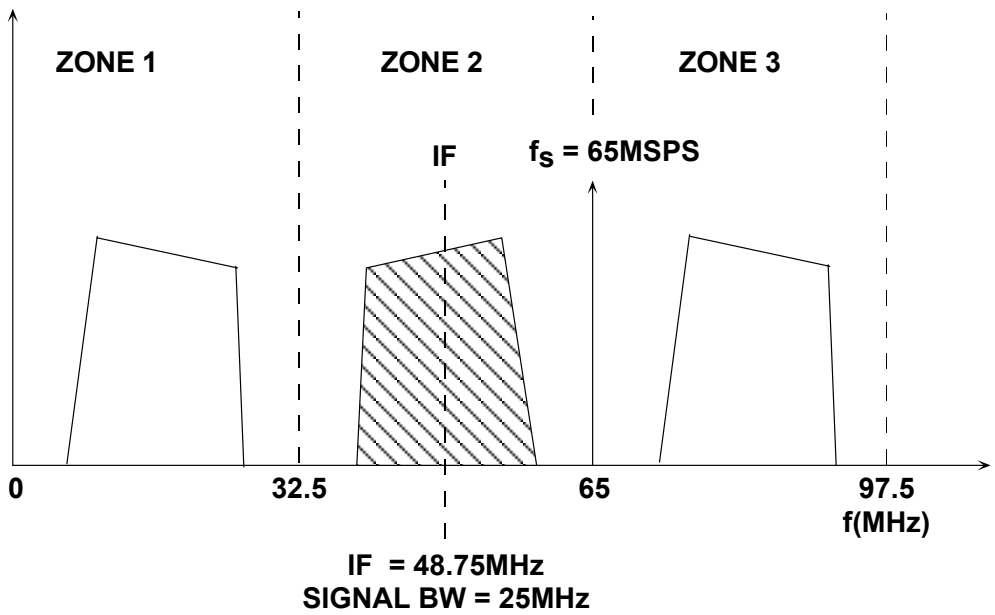


Figure 8.128*: Sampling a 25-MHz BW Signal Using AD6645: IF Frequency = 48.75 MHz, f_s = 65 MSPS*

Figure 8.129 summarizes most of the current (2004) air standards and the approximate ADC requirements based on the individual standard specifications for maximum signal level, minimum signal level, etc. Notice that ADCs are currently available which will meet all the standards except for the GSM 900 MHz systems, previously discussed.

	MULTIPLE ACCESS METHOD	CHANNEL SPACING (BW)	TYPICAL TOTAL BW	ADC SAMPLING RATE (TYP.)	ADC SFDR	ADC SNR
AMPS	FDMA	30kHz	12.5MHz	61.44MSPS	96dBc	72dBFS
IS-136	TDMA/FDM	30kHz	5-15MHz	61-92MSPS	88dBc	68dBFS
GSM 900 MHz	TDMA/FDM	200kHz	5-15MHz	61-92MSPS	106dBc	85dBFS
GSM 1800/1900MHz, PCS	TDMA/FDM	200kHz	5-15MHz	61-92MSPS	93dBc	75dBFS
IS-95	CDMA	1.25MHz	5-15MHz	61-92MSPS	83dBc	74dBFS
CDMA2000	CDMA	1.25MHz	5-15MHz	61-92MSPS	79dBc	74dBFS
WCDMA (UMTS)	CDMA	5MHz	5-20MHz	61-92MSPS	79dBc	69dBFS

Figure 8.129: *Approximate Wideband ADC Requirements for Popular Wireless Air Interface Standards*

Increasing ADC Dynamic Range Using Dither

There are two fundamental limitations to maximizing SFDR in a high speed ADC. The first is the distortion produced by the front-end amplifier and the sample-and-hold circuit. The second is that produced by non-linearity in the actual transfer function of the encoder portion of the ADC. The key to high SFDR is to minimize the non-linearity of each.

There is nothing that can be done externally to the ADC to significantly reduce the inherent distortion caused by the ADC front end. However, the nonlinearity in the ADC encoder transfer function can be reduced by the proper use of dither (external noise which is summed with the analog input signal to the ADC).

Dithering improves ADC SFDR under certain conditions (References 20-23). For example, even in a perfect ADC, there is some correlation between the quantization noise and the input signal. This can reduce the SFDR of the ADC, especially if the input signal is an exact sub-multiple of the sampling frequency. Summing broadband noise (about ½ LSB rms in amplitude) with the input signal tends to randomize the quantization noise and minimize this effect (see Figure 8.130A). In most systems, however, there is enough noise riding on top of the signal so that adding additional dither noise is not required. Increasing the wideband rms noise level beyond an LSB will proportionally reduce the ADC SNR.

Other schemes have been developed which use larger amounts of dither noise to randomize the transfer function of the ADC. Figure 8.130B also shows a dither noise source comprised of a pseudo-random number generator which drives a DAC. This signal is subtracted from the ADC input signal and then digitally added to the ADC output, thereby causing no significant degradation in SNR. An inherent disadvantage of this technique is that the allowable input signal swing is reduced as the amplitude of the dither signal is increased. This reduction in signal amplitude is required to prevent overdriving the ADC. It should be noted that this scheme does not significantly improve

distortion created by the front-end of the ADC, only that produced by the non-linearity of the ADC encoder transfer function.

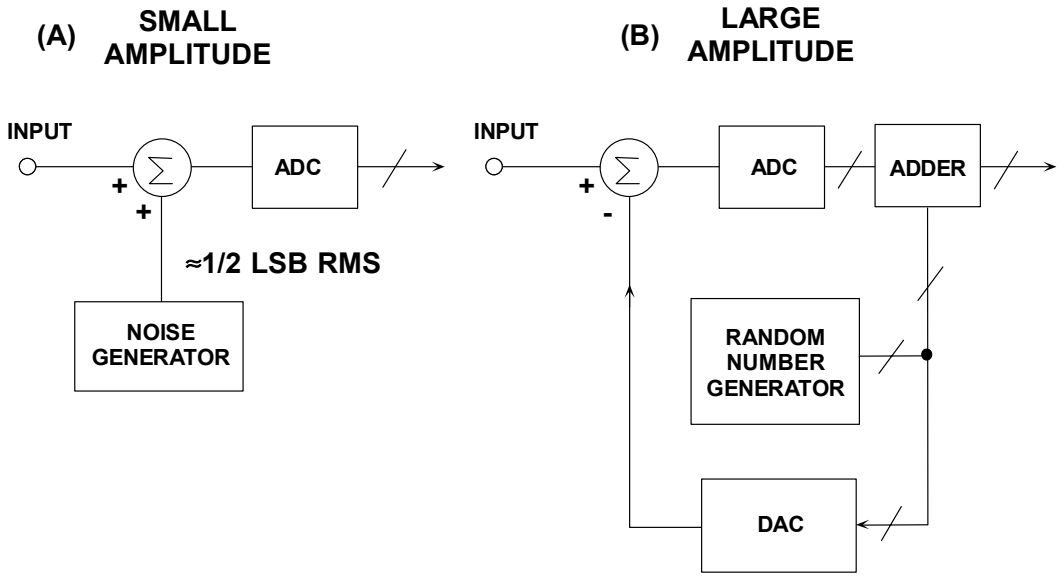


Figure 8.130: *Using Dither to Randomize ADC Transfer Function*

Another method which is easier to implement, especially in wideband receivers, is to inject a narrowband dither signal *outside the signal band of interest* as shown in Figure 8.131. Usually, there are no signal components located in the frequency range near dc, so this low-frequency region is often used for such a dither signal. Another possible location for the dither signal is slightly below $f_S/2$. Because the dither signal occupies only a small bandwidth relative to the signal bandwidth, there is no significant degradation in SNR, as would occur if the dither was broadband.

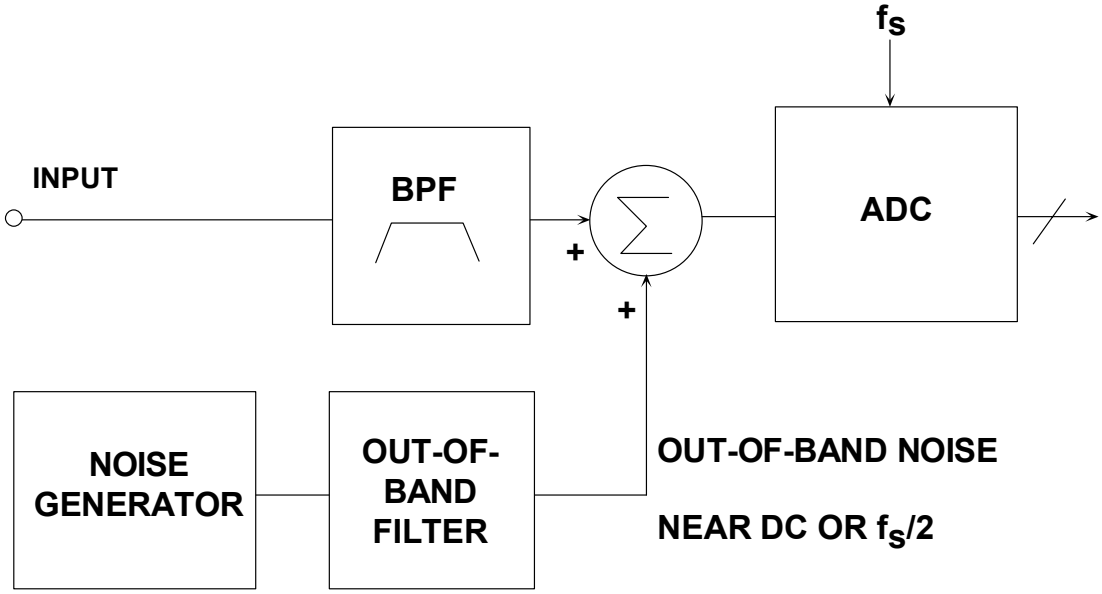


Figure 8.131: *Injecting Out-of-Band Dither to Improve ADC SFDR*

A subranging pipelined ADC, such as the AD6645 (see Figure 8.132), has small differential non-linearity errors that occur at specific regions across the ADC range. The AD6645 uses a 5-bit ADC (ADC1) followed by a 5-bit ADC2 and a 6-bit ADC3. The only significant DNL errors occur at the ADC1 transition points—the second and third stage ADC DNL errors are minimal. There are $2^5 = 32$ decision points associated with ADC1, and they occur every 68.75-mV ($2^9 = 512$ LSBs) for a 2.2-V fullscale input range. Figure 8.133 shows a greatly exaggerated representation of these nonlinearities.

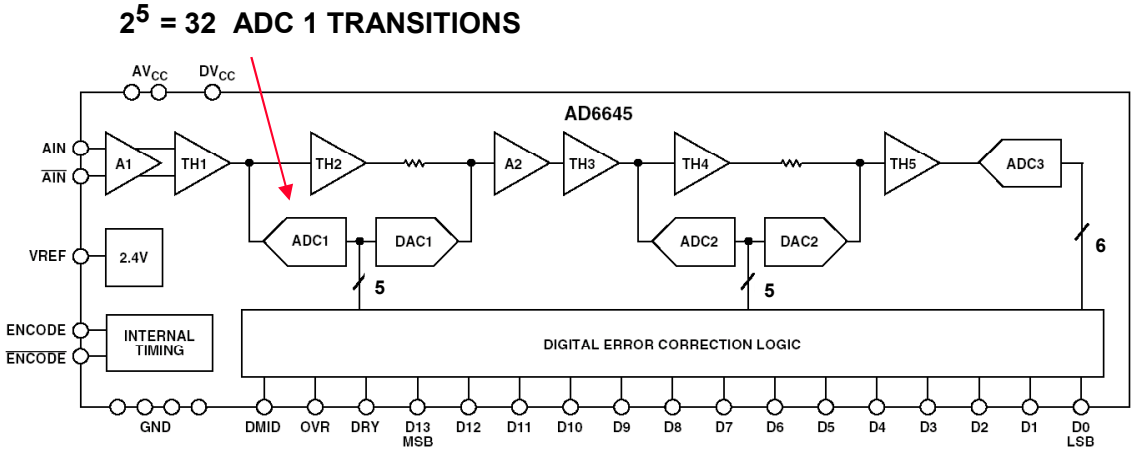


Figure 8.132: *AD6645 Subranging Point DNL Errors (Exaggerated)*

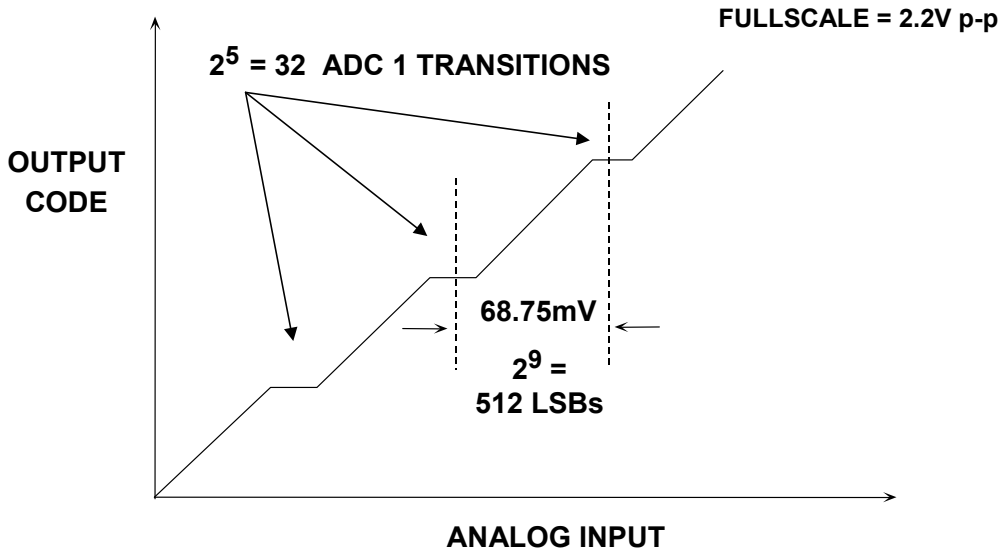


Figure 8.133: *AD6645 Undithered and Dithered DNL*

The distortion components produced by the front end of the AD6645 up to about 200-MHz analog input are negligible compared to those produced by the encoder. That is, *the static non-linearity of the AD6645 transfer function* is the chief limitation to SFDR.

The goal is to select the proper amount of out-of-band dither so that the effect of these small DNL errors are *randomized* across the ADC input range, thereby reducing the average DNL error. Experimentally, it was determined that making the peak-to-peak dither noise cover about two ADC1 transitions gives the best improvement in DNL. The DNL is not significantly improved with higher levels of noise. Two ADC1 transitions cover 1024 LSBs peak-to-peak, or approximately 155 LSBs rms (peak-to-peak gaussian noise is converted to rms by dividing by 6.6).

The first plot shown in Figure 8.134 shows the undithered DNL over a small portion of the input signal range. The horizontal axis has been expanded to show two of the subranging points which are spaced 68.75-mV (512 LSBs) apart. The second plot shows the DNL after adding 155 LSBs rms dither. This amount of dither corresponds to approximately –20.6 dBm. Note the dramatic improvement in the DNL.

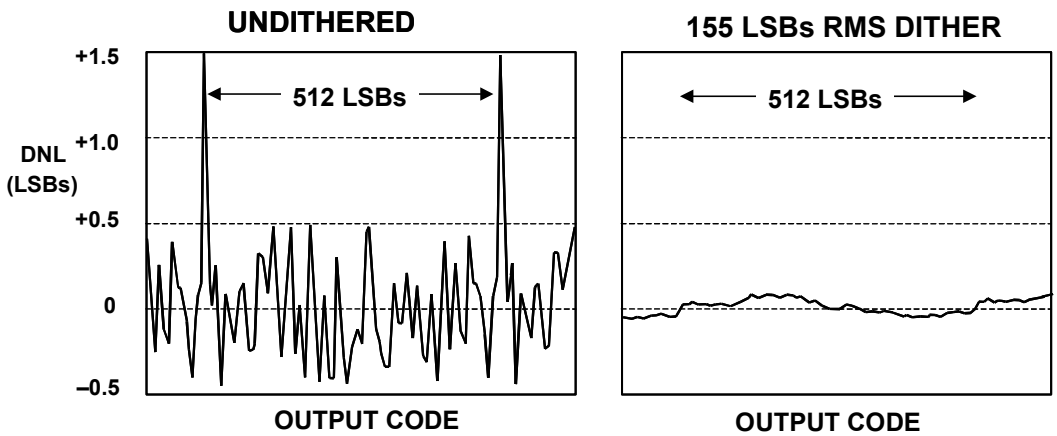


Figure 8.134: *AD6645 Undithered and Dithered DNL*

Dither noise can be generated in a number of ways. Noise diodes can be used, but simply amplifying the input voltage noise of a wideband bipolar op amp provides a more economical solution. This approach has been described in detail (References 21-23) and will not be repeated here.

The dramatic improvement in SFDR obtained with out-of-band dither is shown in Figure 8.135 using a deep (1,048,576-point) FFT, where the AD6645 is sampling a –35-dBm, 30.5-MHz signal at 80 MSPS. Note that the SFDR without dither is approximately 92 dBFS compared to 108 dBFS with dither, representing a 16-dB improvement! Figure 8.136 shows undithered and dithered SFDR as a function of input signal level and again shows the dramatic improvement.

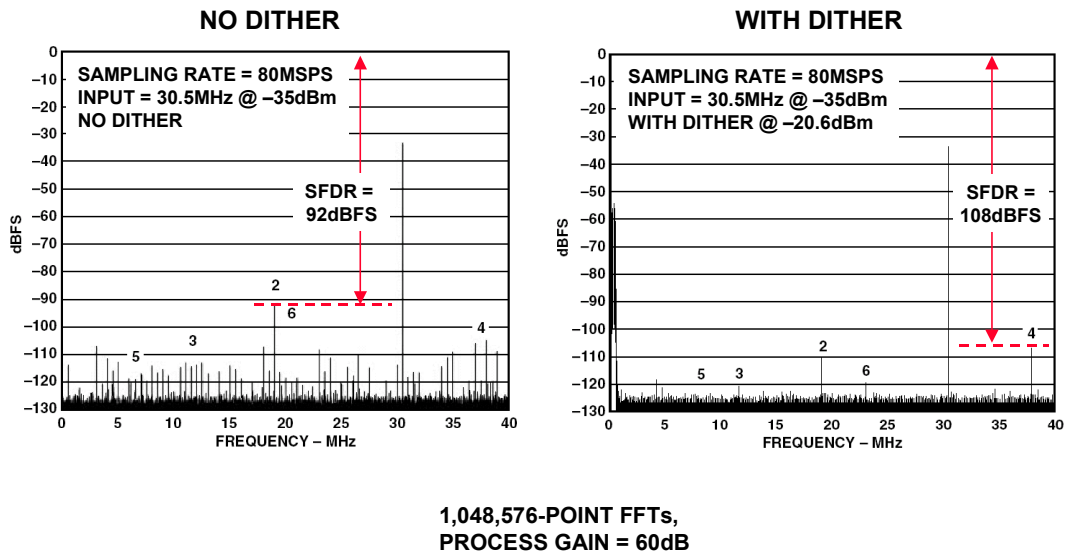


Figure 8.135: *AD6645 Undithered and Dithered SFDR FFT Plot*

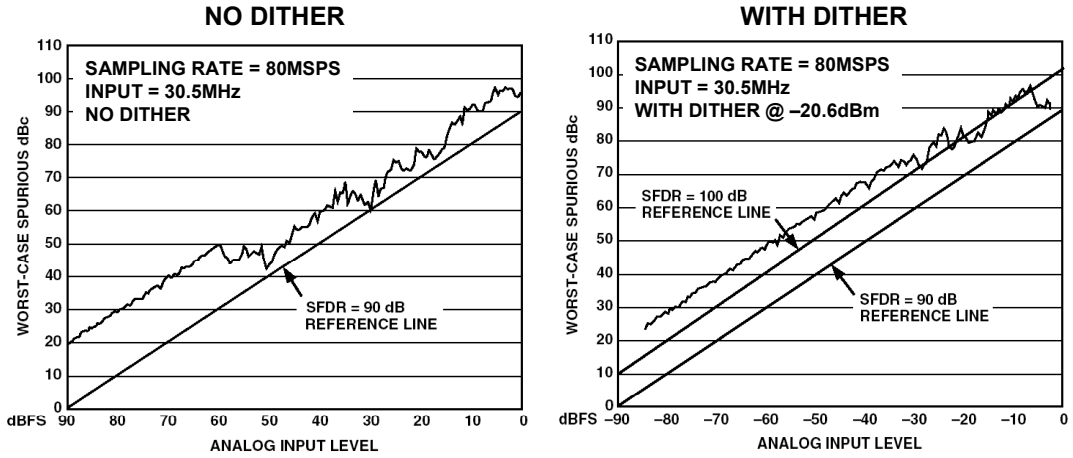


Figure 8.136: *AD6645 Undithered and Dithered SFDR*

We conclude the discussion of single and multicarrier software receivers with a few current (2004) roadmaps of the receiver products available from Analog Devices. The single-carrier family is shown in Figure 8.137, and the multicarrier family in Figure 8.138.

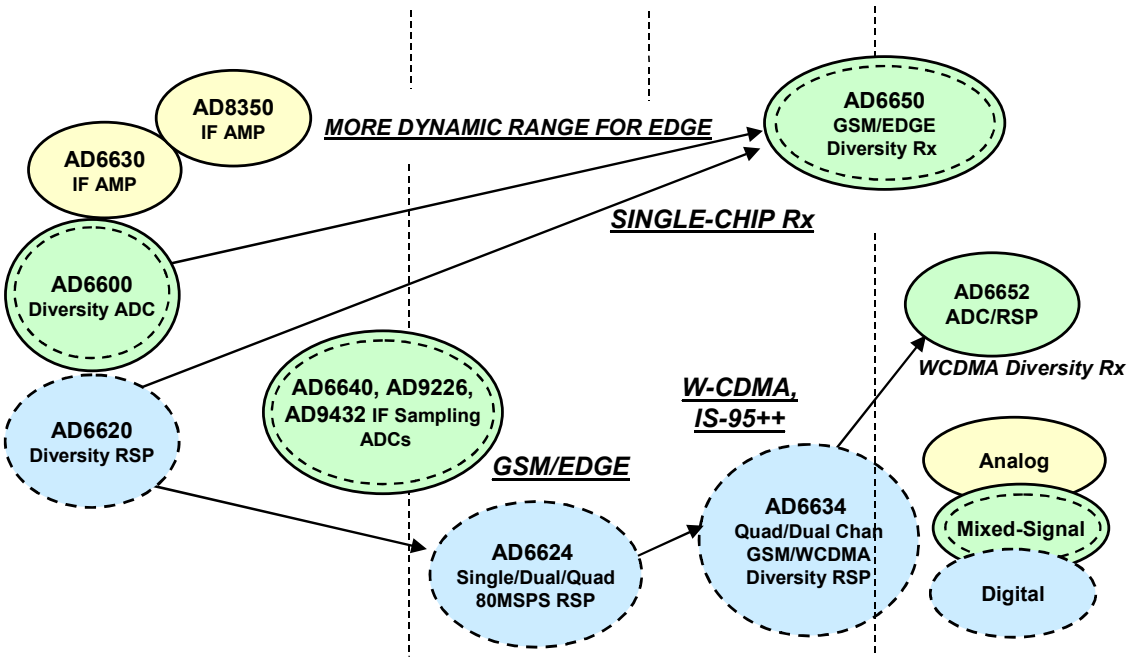


Figure 8.137: *Summary: Single Carrier Receivers*

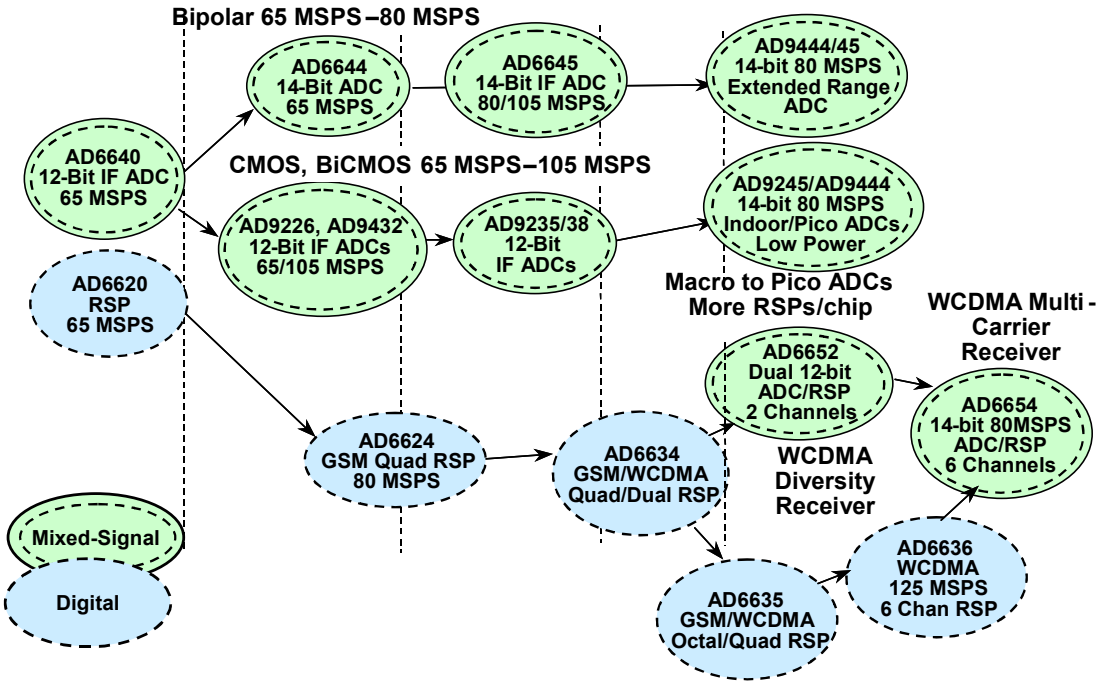


Figure 8.138: *Summary: Multicarrier Receivers*

Wideband Radio Transmitter Considerations

Many of the same concepts discussed in the previous wideband receiver sections apply to wideband transmitters as well. Two basic transmit architectures are shown in 8.139. In quadrature-based modulation schemes, such as QPSK and QAM, mixers are used to mix the in-phase (I) and quadrature (Q-90 degree out of phase) signals into a composite single-sideband signal for transmission. Figure 8.139A demonstrates a baseband transmit architecture that performs an analog mix of the I and Q. In this example, two DACs are required per transmit channel. This is the traditional architecture used in single-carrier systems. Even at the low output frequencies used in many baseband applications, the TxDAC family are the best choice because all family members combine (1) high SFDR at low output frequencies; (2) low power consumption, single-supply operation to enhance system power efficiency; (3) lower overall cost by oversampling the signal (interpolation) to reduce the DACs' in-band aliased images, thus easing the complexity of the analog bandpass filter; and (4) the variety of resolutions offered in the same pin-out allows ultimate cost/performance trade-offs. For example, in many of the TxDAC beta-site applications, users started with one resolution model and later designed-in either a higher- or lower-resolution device based on actual system performance. Details of the TxDAC family can be found in References 24 and 25.

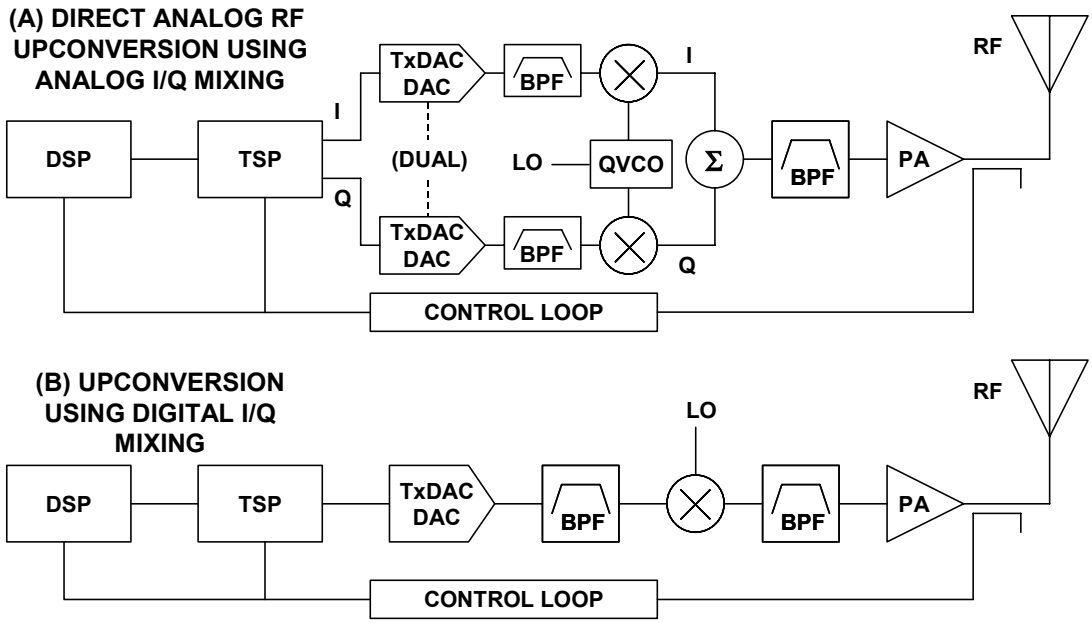


Figure 8.139: *Simplified Wireless Transmitter Architectures*

The system architecture in Figure 8.139B uses digital mixing of I and Q signals within the transmit signal processor (TSP) and sends the modulated signal directly to a single DAC. In this case, the bandwidth requirements of the DAC are more stringent. This approach is best for multicarrier systems. Current TxDACs can receive data at up to 160 MSPS. With digital modulation, intermediate frequencies (IFs) up to 70 MHz can be generated using TxDAC chips. Here, too, high SFDR, low price, low power, and family pin-compatibility are desirable (required) attributes. If multiple digital I and Q modulators are fed into the single DAC depicted in Figure 8.139B, the system becomes a

wideband multicarrier transmit architecture, for which the superior multi-tone performance of the TxDAC family of products is a major performance attribute.

The transmit signal processor is a numeric post-processor for the DSP. The purpose of the TSP is to replace the first local oscillator, quadrature modulator, channel filtering and data interpolation. Like the RSP in the receiver, the TSP sets the transmitter apart from traditional designs because all channel characteristics are now programmable. This includes data rate, channel bandwidth and channel shape. Since modulation, channel filtering and other aspects of the modulation are done digitally, the filters will always perform exactly alike across all boards, unlike analog solutions that always have tolerances.

There are several specifications that are important when selecting a TSP. First, the device must be capable of generating data at the rates required to preserve the Nyquist bandwidth over the spectrum of interest. As with the ADC's sample rate, the sample rate of the DAC determines how much spectrum can be faithfully generated. Therefore, the TSP must be capable of generating data at least twice as fast as the band of interest and preferably three times faster as reasoned earlier for antialiasing filter response.

Similar to RSPs, the bus widths are also important, yet for different reasons. In the transmit direction, there are two different issues. If the TSP is used in a single-channel mode, then the issue is simply quantization and thermal noise. It is usually not desirable to transmit excess in-band or out-of-band noise, since this wastes valuable transmitter efficiency and causes interference. In a multicarrier application, the concern is slightly different. Here, many channels would be digitally summed before reconstruction with a D/A converter. Therefore, each time the number of channels is doubled, an additional bit should be added so that the dynamic range is not taken from one channel when another is added.

Finally, the ability to frequency hop is vital. Since a TSP implements frequency control with an NCO and a mixer, frequency hopping can be very fast, allowing the implementation of the most demanding hopping applications as found in the GSM specification.

Basically, a DAC is similar to an ADC when considering performance requirements. Therefore, the first specification of interest is the signal-to-noise ratio. As with an ADC, SNR is primarily determined by quantization and thermal noise. If either is too large, then the noise figure of the DAC will begin to contribute to the overall signal chain noise. While noise is not necessarily a concern spectrally, the issue does become important when the DAC is used to reconstruct multiple signals. In this case, the DAC output signal swing ("power") is shared among the carriers. The theoretical SNR of a DAC is determined by the same set of equations that govern ADC, and the noise figure can be derived given a specific SNR.

The AD9786 is one of the latest TxDACs suitable for a variety of air standards. A simplified block diagram is shown in Figure 8.140. The device accepts I and Q input data at a rate up to 160 MSPS, and provides on-chip interpolation of 2, 4, and 8. I and Q modulation is performed digitally within the device. The interpolated output sampling rate can be as high as 400 MSPS. Direct IF output frequencies up to 70 MHz are possible.

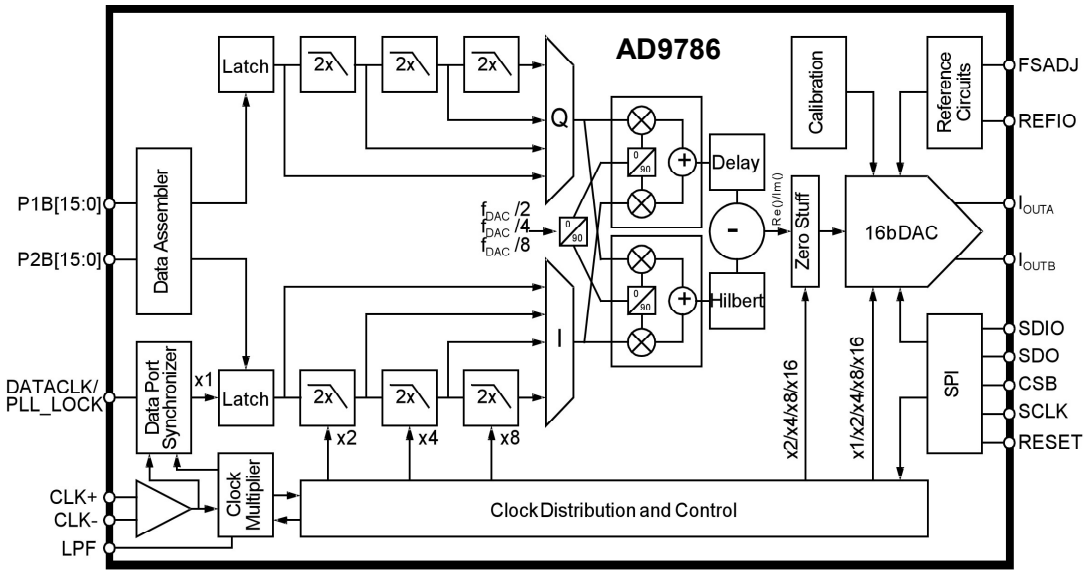


Figure 8.140: *AD9786 16-Bit, 160-MSPS TxDAC+® with 2×/4×/8× Interpolation and Signal Processing*

As explained in Chapter 2, oversampling by interpolation relaxes the requirements on the anti-imaging output filter as well as reduces the effects of "sin x/x" rolloff.

The AD9786 has a noise floor of –163 dBm/Hz up to 100 MHz. IMD performance to 300 MHz is less than –80 dBc, and 10-MHz SFDR is 90 dBc. These and other key specifications are summarized in Figure 8.141. Overall performance is more than sufficient to meet the exacting transmitter requirements of all multicarrier air standards, including GSM and WCDMA. A summary of the TxDAC family is shown in Figure 8.142. Figure 8.143 shows a summary of the entire Analog Devices' receiver and transmitter "Softcell" family.

For applications requiring analog I/Q modulation, the AD8349 is a silicon monolithic RF IC quadrature modulator, designed for use from 0.8 GHz to 2.7 GHz. Its excellent phase accuracy and amplitude balance enable high performance direct RF modulation. A functional diagram is shown in Figure 8.144. The differential LO signal first passes through a polyphase phase splitter. The I- and Q-channel outputs of the phase splitter are buffered to drive the LO inputs of two Gilbert cell mixers. Two differential V-to-I converters connected to the I- and Q-channel baseband inputs provide the tail currents for the mixers. The outputs of the two mixers are summed together by a differential buffer to drive 50-Ω loads. The device also features an output disable function. The AD8349 can be used as a direct-to-RF transmit modulator in digital communication systems such as GSM, CDMA, WCDMA basestations and QPSK or QAM broadband wireless access transmitters. It can also be used as the IF modulator within LMDS transmitters. Additionally, this quadrature modulator can be used with direct digital synthesizers in hybrid phase-locked loops to generate signals over a wide frequency range with millihertz resolution. The AD8349 is supplied in a 16-lead exposed-paddle TSSOP

package. Its performance is specified over a –40°C to +85°C temperature range. This device is fabricated on Analog Devices' advanced complementary silicon bipolar process.

- **Targeted at the most demanding Multi-Carrier Macro GSM/WCDMA basestation applications**
- **16-/14-/12-Bit resolution with up to 400MSPS DAC Update Rate**
- **Selectable 2×/4×/8× High Performance Interpolation filters 160MSPS Data Rate**
- **Direct IF Transmission Frequencies 70MHz and Higher**
- **2's Complement/Straight Binary Selectable Data Format**
- **LVTTL/CMOS Compatible Inputs**
- **Programmable via SPI Port**
- **Noise Floor Performance: –163dBm/Hz out to 100MHz**
- **IMD to 300MHz: < –80dBc**
- **SFDR @ 10MHz: 90dBc**
- **Versatile Clock Interface**
- **Power Dissipation: ~800mW, Single Supply (+2.5 V / +3 V)**
- **80 pin LQFP Package**

Figure 8.141: *AD978x 16-Bit Interpolating TxDAC+ Family Key Specifications*

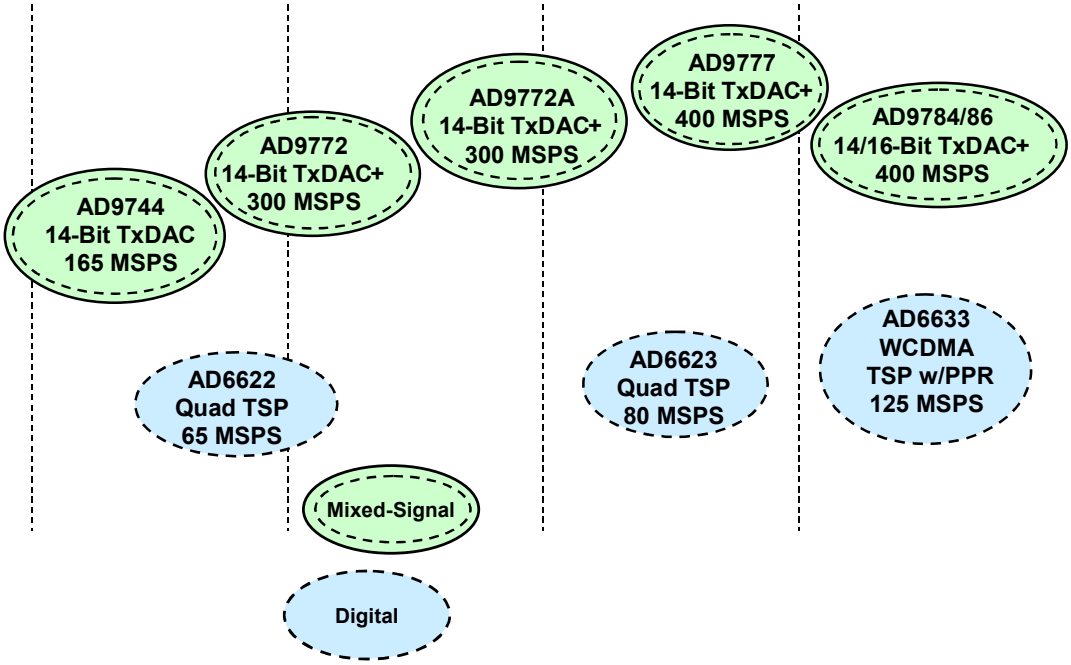


Figure 8.142: *Multicarrier Transmitters*

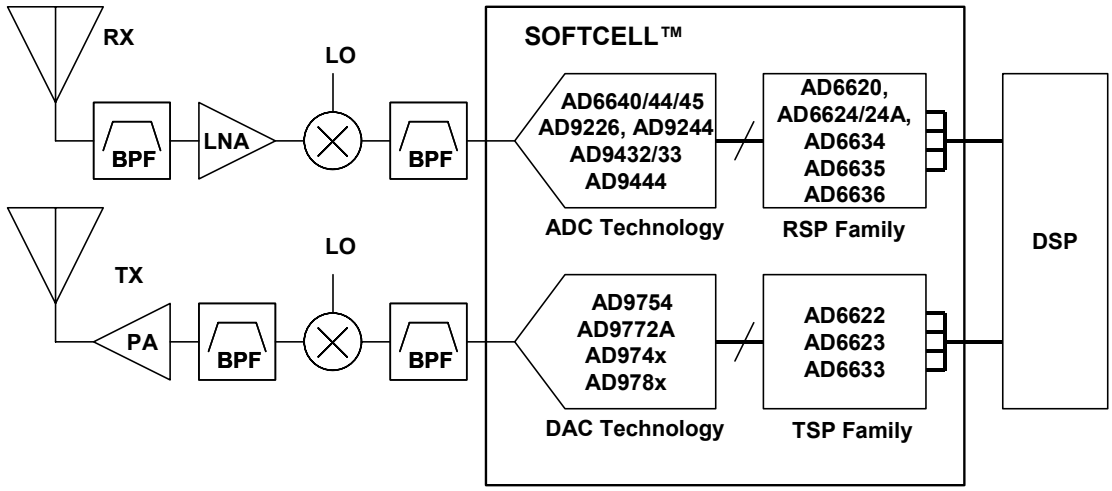


Figure 8.143: *Multicarrier Transceiver Summary*

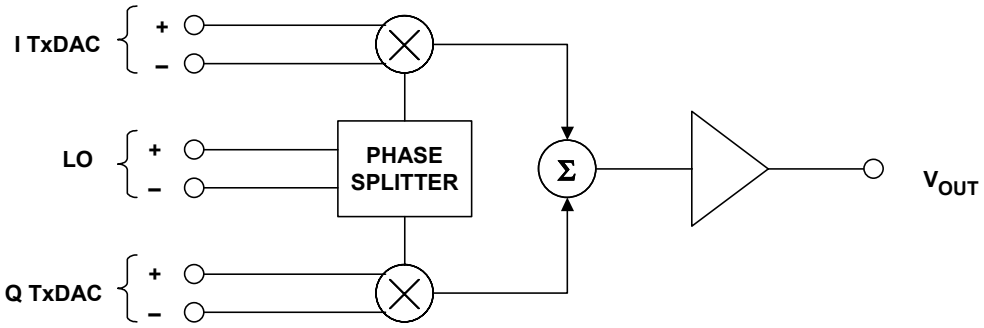


Figure 8.144: *AD8349 800-MHz to 2.7-GHz Quadrature Modulator*

Cellular Telephone Handsets

One of the fastest growing and rapidly changing high volume applications of digital radio is the cellular telephone handset. Each new generation of handsets has a lower components count, lower power, and more features than the previous models. Because of the different air standards, multimode and multiband operation is required. In order to give an overview of the cellular telephone handset, we will limit the discussion to GSM—with the additional understanding that the product examples shown do not necessarily represent the latest generation Analog Devices' product offerings due to proprietary considerations.

Figure 8.145 shows a simplified block diagram of the GSM Digital Cellular Telephone System. The *speech encoder and decoder* and *discontinuous transmission* function will be described in detail. Up conversion and downconversion portions of the system contain mixed signal functions and will be described later. Similar functions are performed

digitally such as equalization, convolutional coding, Viterbi decoding, modulation and demodulation.

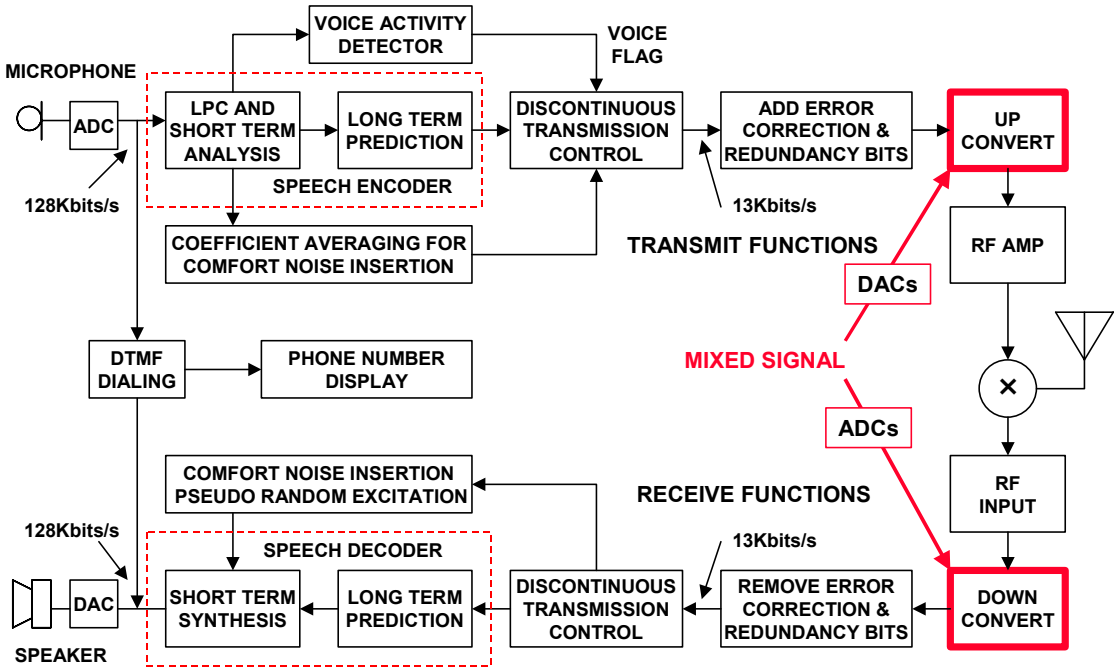


Figure 8.145: *GSM Handset Block Diagram*

The standard for encoding voice signals has been set in the T-Carrier digital transmission system. In this system, speech is logarithmically encoded to 8 bits at a sampling rate of 8 kSPS. The logarithmic encoding and decoding to 8 bits is equivalent to linear encoding and decoding to 13-bits of resolution. This produces a bit-rate of 104 kb/s. In most handsets, a 16-bit Σ-Δ ADC is used, so the effective bit-rate is 128 kb/s. The Speech Encoder portion of the GSM system compresses the speech signal to 13 kb/s, and the decoder expands the compressed signal at the receiver. The speech encoder is based on an enhanced version of linear predictive coding (LPC). The LPC algorithm uses a model of the human vocal tract that represents the throat as a series of concentric cylinders of various diameters. An excitation (breath) is forced into the cylinders. This model can be mathematically represented by a series of simultaneous equations which describe the cylinders.

The excitation signal is passed through the cylinders, producing an output signal. In the human body, the excitation signal is air moving over the vocal cords or through a constriction in the vocal tract. In a digital system, the excitation signal is a series of pulses for vocal excitation, or noise for a constriction. The signal is input to a digital lattice filter. Each filter coefficient represents the size of a cylinder.

An LPC system is characterized by the number of cylinders it uses in the model. Eight cylinders are used in the GSM system, and eight reflection coefficients must be generated.

Early LPC systems worked well enough to understand the encoded speech, but often the quality was too poor to recognize the voice of the speaker. The GSM LPC system

employs two advanced techniques that improve the quality of the encoded speech. These techniques are *regular pulse excitation* (RPE) and *long term prediction* (LTP). When these techniques are used, the resulting quality of encoded speech is nearly equal to that of logarithmic pulse code modulation (companded PCM as in the T-Carrier system).

The actual input to the speech encoder is a series of 16-bit samples of uniform PCM speech data. The sampling rate is 8 kSPS. The speech encoder operates on a 20-ms window (160 samples) and reduces it to 76 coefficients (260 bits total), resulting in an encoded data rate of 13 kb/s.

Discontinuous transmission (DTX) allows the system to shut off transmission during the pauses between words. This reduces transmitter power consumption and increases the overall GSM system's capacity.

Low power consumption prolongs battery life in the handset and is an important consideration for hand-held portable phones. Call capacity is increased by reducing the interference between channels, leading to better spectral efficiency. In a typical conversation each speaker talks for less than 40% of the time, and it has been estimated that DTX can approximately double the call capacity of the radio system.

The voice activity detector (VAD) is located at the transmitter. Its job is to distinguish between speech superimposed on the background noise and noise with no speech present. The input to the voice activity detector is a set of parameters computed by the speech encoder. The VAD uses this information to decide whether or not each 20-ms frame of the encoder contains speech.

Comfort noise insertion (CNI) is performed at the receiver. The comfort noise is generated when the DTX has switched off the transmitter; it is similar in amplitude and spectrum to the background noise at the transmitter. The purpose of the CNI is to eliminate the unpleasant effect of switching between speech with noise, and silence. If you were listening to a transmission without CNI, you would hear rapid alternating between speech in a high-noise background (i.e. in a car), and silence. This effect greatly reduces the intelligibility of the conversation.

When DTX is in operation, each burst of speech is transmitted followed by a *silence descriptor* (SID) frame before the transmission is switched off. The SID serves as an end of speech marker for the receive side. It contains characteristic parameters of the background noise at the transmitter, such as spectrum information derived through the use of linear predictive coding.

The SID frame is used by the receiver's comfort noise generator to obtain a digital filter which, when excited by pseudo-random noise, will produce noise similar to the background noise at the transmitter. This comfort noise is inserted into the gaps between received speech bursts. The comfort noise characteristics are updated at regular intervals by the transmission of SID frames during speech pauses.

Redundant bits are then added by the processor for error detection and correction at the receiver, increasing the final encoded bit rate to 22.8 kb/s. The bits within one window,

and their redundant bits, are interleaved and spread across several windows for robustness.

The Role of ADCs and DACs in Cellular Telephone Handsets
Doug Grant

The cell phone handset uses quite a bit of ADC and DAC technology. Starting with the audio section, we find a high-performance voiceband codec. Unlike the companded voice codecs used in the public switched telephone network, the voice codecs used in cellular handsets are linear-coded and higher resolution, typically 16 bits. Linear coding is preferred, because all cellular systems use DSP compression algorithms to reduce the bit rate to be transmitted, and the math is simpler when linear coding is used. Furthermore, less information is lost in the mathematical operations with linear coding, and this SNR is better than typical companded voiceband codecs.

The voiceband ADCs in cell phones are all Σ-Δ types, and include digital filters compliant with the bandwidth and stopband-rejection specs dictated by the applicable standard. In GSM, these converters provide 16-bit resolution, 8-kSPS sample rates, and 60-dB to70-dB signal-to-noise ratio in the voice band. The ADC section also includes analog interfaces to accommodate a variety of microphone types, with dc bias for electret types, single-ended and differential inputs, programmable gain, switch hook detection, etc., as well as other sources such as built in FM radio or MP3 decoders. The DAC section includes audio output driver amplifiers suitable for speakers, earpieces, and headphones of various types and impedances, as well as provision for mixing multiple audio sources to an output device. And of course, they are optimized for low-voltage and low-power operation, with efficient power-up and power-down sequencing to save battery life.

Some advanced handsets now include higher-performance DACs to enable playback of ringing and game tones, MP3 audio clips, and even full streaming audio content. These include all the usual features of multi-standard audio playback converters, such as sample-rate conversion, but again with the constraints of low voltage, low current drain, and efficient power-up/power-down sequencing.

Converters also play an important part in the radio and baseband signal chain. Most cellular handsets down-convert the modulated RF signal to quadrature (I/Q) baseband components. In order to process these signals, dual Σ-Δ A/D converters are generally used, with integrated digital channel selection filters matched to the transmitted waveform for maximum transfer of signal energy. On the transmit side, most systems calculate the quadrature components of the waveform representing the bit stream to be transmitted, and load the waveforms in a burst RAM prior to transmission. At the appointed time, the RAM contents are clocked into a pair of DACs which modulate an intermediate-frequency carrier which is then upconverted to the appropriate RF carrier frequency, or in some implementations, the DACs modulate the carrier directly. The converter requirements in such a system are dictated by the tradeoff of analog and digital filtering used in the system, signal bandwidth, dc offsets in the receive path before the ADCs, and the required signal-to-noise ratio to support the bit-error-rate needed for the system. In a typical GSM/GPRS/EDGE handset, the ADCs are on the order of 16-bit resolution with 65-dB to 75-dB dynamic range and sample rates equal to the symbol rate

(270.833 kSPS). And of course, these system-specific parameters are in addition to the general requirements in a handset for low-voltage, low-current operation, with efficient control of power-up and power-down sequencing.

Cellular handsets also include several additional converters of varying resolutions and speeds for the monitoring and control of handset functions. Some of these functions include battery status and charge control, battery and power amplifier (PA) temperature monitoring, receive-path gain and offset control, transmit burst power ramp-up/down, automatic frequency control, and display brightness control. Most of these functions only require converters with relatively low bandwidth and low-to-moderate (10- to 14-bit) resolution.

SoftFone and Othello Radio Chipsets from Analog Devices
(The following descriptions of the Othello Radio chipsets do not reflect the latest generation Analog Devices' products. Details of the latest generation designs are available from Analog Devices under non-disclosure agreeement.)

Analog Devices offers a chipset which comprises the majority of a GSM handset. The SoftFone® chipset performs the baseband and DSP functions, while the Othello® radio chipset handles the RF functions as shown in Figure 8.146.

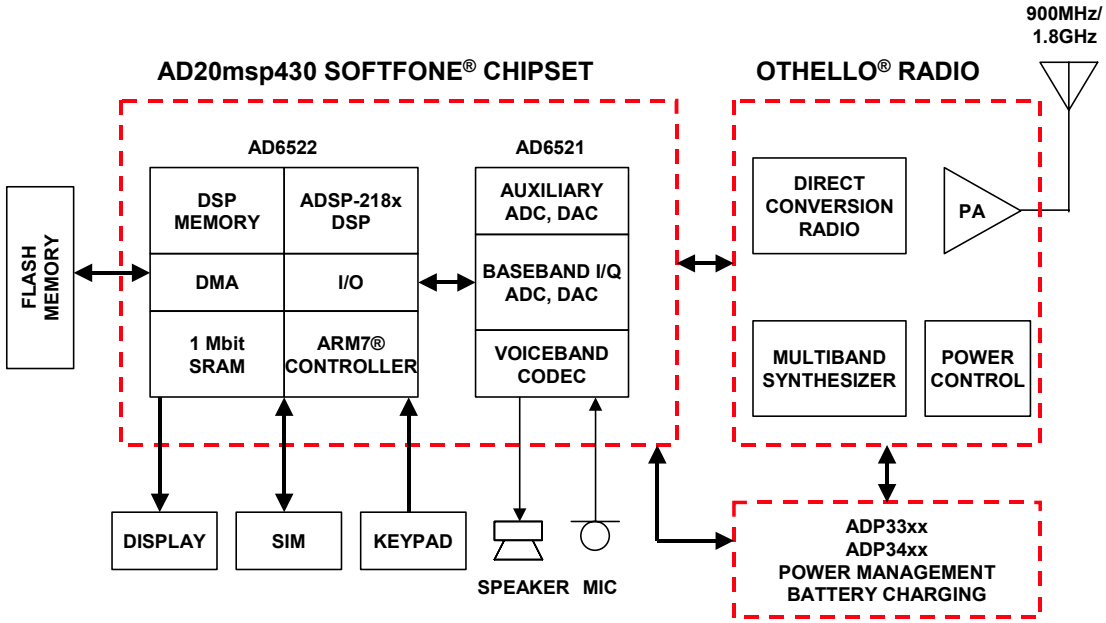


Figure 8.146: *Othello® Radio and SoftFone® Chipsets Make Complete GSM/DCS Handset*

Because of the frequency allocations in GSM countries (other than the U.S.), most GSM handsets must be dual-band: capable of handling both GSM and DCS frequencies. The SoftFone® and Othello® chipsets supply the main functions necessary for implementing dual- or triple-band radios for GSM cellular phones. The AD20msp430 SoftFone® chipset comprises the baseband portion of the GSM handset. The AD20msp430 baseband processing chipset uses a combination of GSM system knowledge and advanced analog and digital signal processing technology to provide a new benchmark in GSM/GPRS

terminal design. The SoftFone architecture is entirely RAM-based. The software is loaded from FLASH memory and is executed from the on-chip RAM. This allows fast development cycles, since no ROM-code turns are required. Furthermore, the handset software can be updated in the field to enable new features. Combined with the Analog Devices Othello RF chipset, a complete multiband handset design contains less than 200 components, fits in a 20 cm^2 single sided PCB layout, and has a total bill-of-materials cost 20-30% lower than previous solutions.

The AD20msp430 chipset is comprised of two chips, the AD6522 DSP-based baseband processor and the AD6521 voiceband/baseband mixed-signal codec. Together with the Othello radio, the AD20msp430 allows a significant reduction in the component count and bill-of-materials (BOM) cost of GSM voice handsets and data terminals. The software and hardware foundations of the AD20msp430 chipset enjoy a long history of successful integration into GSM handsets. This is Analog Devices' 4th generation of GSM chipsets, each of which has passed numerous type- approvals and network operator approvals in OEM handsets. In each generation, additional features have been added, while cost and power have been reduced. Numerous power-saving features have been included in the AD20msp430 chipset to reduce the total power consumption. A programmable state machine allows events to be controlled with a resolution of one-quarter of a bit period. The AD20msp430 chipset uses the SoftFone® architecture, where all software resides in RAM or FLASH memory. Since ROM is not used, development time is reduced and additional features can be field-installed easily.

There are two processors in the AD20msp430 chipset. The DSP processor is the ADSP-218x core, proven in previous generations of GSM chipsets, and operated at 65 MIPS in the AD20msp430. This DSP performs the voiceband and channel coding functions previously discussed. The AD6521 voiceband/baseband codec chip contains all analog and mixed-signal functions. These include the I/Q channel ADCs and DACs, high performance multichannel voiceband codec, and several auxiliary ADCs and DACs for AGC (automatic gain control), AFC (automatic frequency control), and power- amplifier ramp control. The microcontroller is an ARM7 TDMI, running at 39 MIPS. The ARM7® handles the protocol stack and the man-machine interface functions. Both processors are field-proven in digital wireless applications. A simplified block diagram of the AD6521 baseband/voiceband codec is shown in Figure 8.147.

The AD20msp430 chipset is fully supported by a suite of development tools and software. The development tools allow easy customization of the DSP and/or ARM® controller software to allow handset and terminal manufacturers to optimize the feature set and user interface of the end equipment. Software is available for all layers, including both voice and data applications, and is updated as new features become available. The system DMA and interrupt controllers are designed to allow easy upgrades to future generations of DSP and controller cores. The display interface can be used with either parallel or serial-interface displays. System development can be shortened by the use of the debugging features in the AD20msp430. Most critical signals can be routed under software control to the Universal System Connector. This allows system debugging to take place in the final form factor. In addition, the architecture includes high speed logger and address trace functions in the DSP and single-wire trace/debug in the ARM controller.

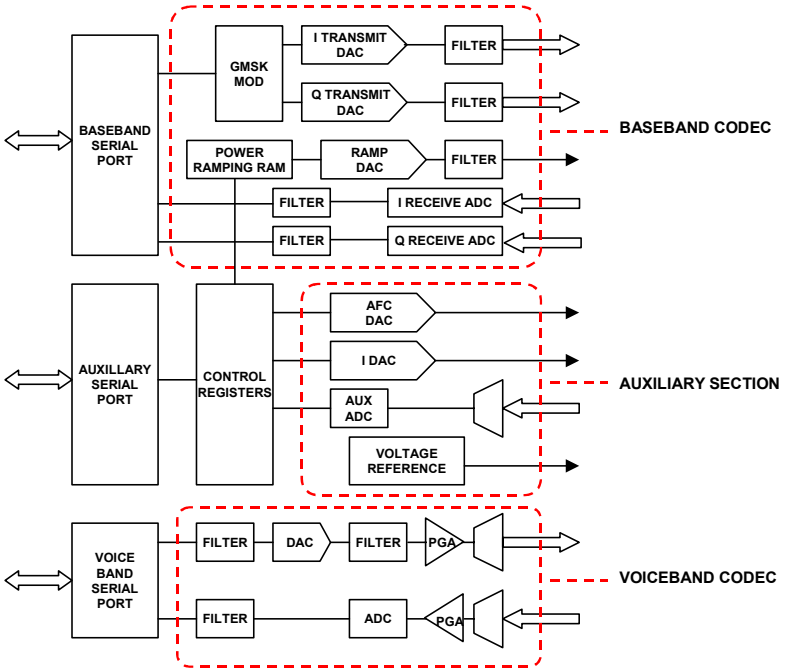


Figure 8.147: *AD6521 Baseband/Voiceband Codec Simplified Block Diagram*

The Analog Devices' Othello® direct-conversion radio eliminates intermediate-frequency (IF) stages, permits the mobile electronics industry to reduce the size and cost of radio sections, and enables flexible, multi-standard, multi-mode operation. The radio includes a Zero-IF Transceiver and a Multi-Band Synthesizer.

Othello contains the main functions necessary for both a direct-conversion receiver and a direct VCO transmitter, known as the Virtual-IF™ transmitter. It also includes the local-oscillator generation block and a complete on-chip regulator that supplies power to all active circuitry for the radio. Also included is a fractional-N synthesizer that features extremely fast lock times to enable advanced data services over cellular telephones-such as high-speed circuit-switched data (HSCSD) and general packet radio services (GPRS).

Most digital cellular phones today include at least one "downconversion" in their signal chain. This frequency conversion shifts the desired signal from the allocated RF band for the standard (say, at 900 MHz) to some lower intermediate frequency (IF), where channel selection is performed with a narrow channel-select filter (usually a surface acoustic-wave (SAW) or a ceramic type). The now-filtered signal is then further down-converted to either a second IF or directly to baseband, where it is digitized and demodulated in a digital signal processor (DSP). Figure 8.148 shows the comparison between this *superheterodyne* architecture and the *superhomodyne*™ architecture of the Othello radio receiver.

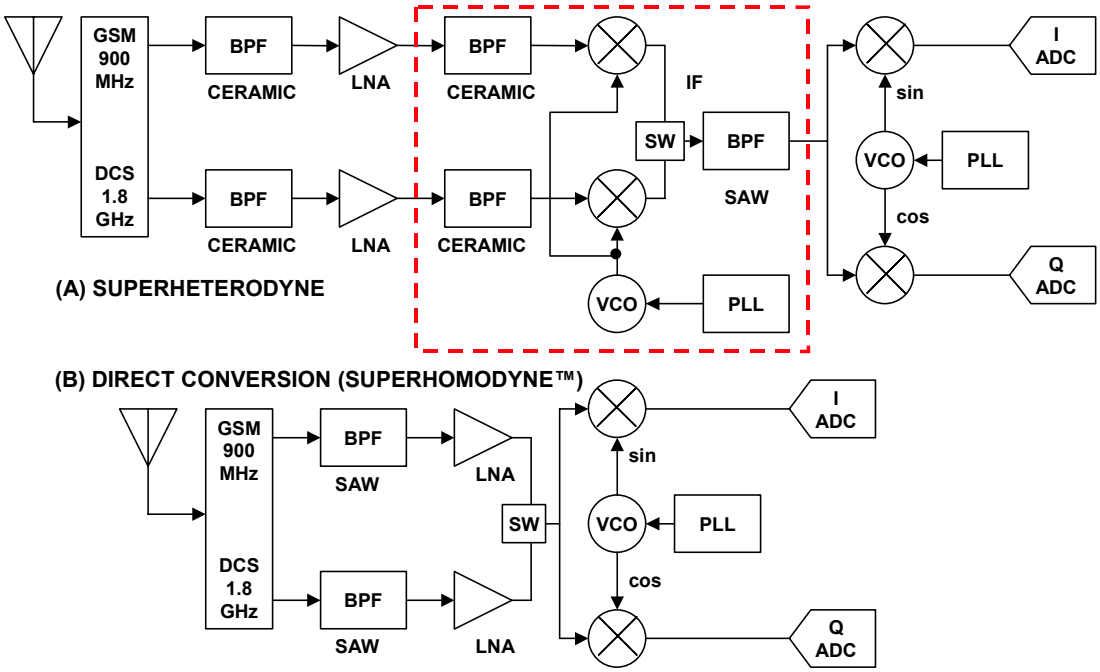


Figure 8.148: *Direct Conversion Receiver Architecture Eliminates Components*

The idea of using direct-conversion for receivers has long been of interest in RF design. The reason is obvious: in consumer equipment conversion stages add cost, bulk, and weight. Each conversion stage requires a local oscillator, (often including a frequency synthesizer to lock the LO onto a given frequency), a mixer, a filter, and (possibly) an amplifier. No wonder, then, that direct conversion receivers would be attractive. All intermediate stages are eliminated, reducing the cost, volume, and weight of the receiver.

The Othello® radio reduces the component count even more by integrating the front-end GSM low-noise amplifier (LNA). This eliminates an RF filter (the "image" filter) that is necessary to eliminate the image, or unwanted mixing product of a mixer and the off chip LNA. This stage, normally implemented with a discrete transistor, plus biasing and matching networks, accounts for a total of about 12 components. Integrating the LNA saves a total of about 15 to 17 components, depending on the amount of matching called for by the (now-eliminated) filter.

A simplified functional block diagram of the Othello® dual band GSM radio's architecture is shown in Figure 8.149. The receive section is at the top of the figure. From the antenna connector, the desired signal enters the transmit/receive switch and exits on the appropriate path, either 925-960 MHz for the GSM band or 1805-1880 MHz for DCS. The signal then passes through an RF band filter (a so-called "roofing filter") that serves to pass the entire desired frequency band while attenuating all other out-of-band frequencies (blockers-including frequencies in the transmission band) to prevent them from saturating the active components in the radio front end. The roofing filter is followed by the low-noise amplifier (LNA). This is the first gain element in the system, effectively reducing the contribution of all following stages to system noise. After the LNA, the direct-conversion mixer translates the desired signal from radio frequency (RF)

all the way to baseband by multiplying the desired signal with a local oscillator (LO) output at the same frequency.

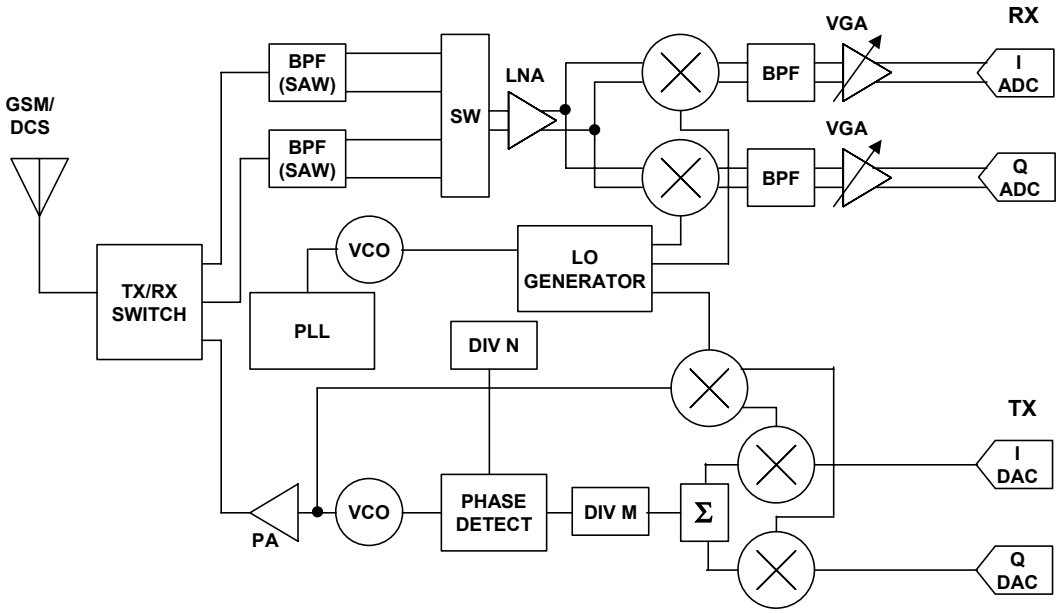


Figure 8.149: *Superhomodyne™ Direct Conversion Dual-Band Transceiver Using Othello*

The output of the mixer stage is then sent in quadrature (I and Q channels) to the variable-gain baseband amplifier stage. The VGA also provides some filtering of adjacent channels, and attenuation of in-band blockers. These blocking signals are other GSM channels that are some distance from the desired channel, say 3 MHz and beyond. The baseband amplifiers filter these signals so that they will not saturate the Receive ADCs. After the amplifier stage, the desired signal is digitized by the Receive ADCs.

The Transmit section begins on the right, at the multiplexed I and Q inputs/outputs. Because the GSM system is a time division duplex (TDD) system, the transmitter and receiver are never on at the same time. The Othello® radio architecture takes advantage of this fact to save four pins on the transceiver IC's package. The quadrature transmit signals enter the transmitter through the multiplexed I/Os. These I and Q signals are then modulated onto a carrier at an intermediate frequency greater than 100 MHz.

The output of the modulator goes to a phase-frequency detector (PFD), where it is compared to a reference frequency that is generated from the external channel selecting LO. The output of the PFD is a charge pump, operating at above 100 MHz, whose output is filtered by a fairly wide (1-MHz) loop filter. The output of the loop filter drives the tuning port of a voltage-controlled oscillator (VCO), with frequency ranges that cover the GSM and DCS transmit bands.

The output of the transmit VCO is sent to two places. The main path is to the transmit power amplifier (PA), which amplifies the transmit signal from about +3 dBm to +35 dBm, sending it to the transmit/receive switch and low pass filter (which attenuates power-amplifier harmonics). The power amplifiers are dual band, with a simple CMOS

control voltage for the band switch. The VCO output also goes to the transmit feedback mixer by means of a coupler, which is either a printed circuit, built with discrete inductors and capacitors, or a monolithic (normally ceramic) coupling device. The feedback mixer downconverts the transmit signal to the transmit IF, and uses it as the local oscillator signal for the transmit modulator. This type of modulator has several names, but the most descriptive is probably "translation loop". The translation loop modulator takes advantage of one key aspect of the GSM standard: the modulation scheme is Gaussian-filtered minimum-shift keying (GMSK). This type of modulation does not affect the envelope amplitude, which means that a power amplifier can be saturated and still not distort the GMSK signal sent through it.

GMSK can be generated in several different ways. In another European standard (for cordless telephones), GMSK is created by directly modulating a free running-VCO with the Gaussian filtered data stream. In GSM, the method of choice has been quadrature modulation. Quadrature modulation creates accurate phase GMSK, but imperfections in the modulator circuit (or up-conversion stages) can produce envelope fluctuations, which can in turn degrade the phase trajectory when amplified by a saturated power amplifier. To avoid such degradations, GSM phone makers have been forced to use amplifiers with somewhat higher linearity, at the cost of reduced efficiency and talk time per battery charge cycle.

The translation loop modulator combines the advantages of directly modulating the VCO and the inherently more accurate quadrature modulation. In effect, the scheme creates a phase locked loop (PLL), comprising the modulator, the LO signal, and the VCO output and feedback mixer. The result is a directly modulated VCO output with a perfectly constant envelope and almost perfect phase trajectory. Phase trajectory errors as low as 1.5 degrees have been measured in Othello, using a signal generator as the LO signal to provide a reference for the loop.

Because Othello® radios can be so compact, they enable GSM radio technology to be incorporated in many products from which it has been excluded, such as very compact phones or PCMCIA cards. However, the real power of direct conversion will be seen when versatile third-generation phones are designed to handle multiple standards. With direct-conversion, hardware channel-selection filters will be unnecessary, because channel selection is performed in the digital signal-processing section, which can be programmed to handle multiple standards. Contrast this with the superheterodyne architecture, where multiple radio circuits are required to handle the different standards (because each will require different channel-selection filters), and all the circuits will have to be crowded into a small space. With direct conversion, the same radio chain could in concept be used for several different standards, bandwidths, and modulation types. Thus, Web-browsing and voice services could, in concept, occur over the GSM network using the same radio in the handset.

Time-Interleaved IF Sampling ADCs with Digital Post-Processors

Mark Looney

The material in this section was extracted from Mark Looney's Analog Dialogue article, Reference 35.

Time interleaving of multiple analog-to-digital converters by multiplexing the outputs of (for example) a pair of converters at a doubled sampling rate is by now a mature concept—first introduced by Black and Hodges in 1980 (Reference 26, 27). While designing a 7-bit, 4-MHz ADC, they determined that a time-interleaved solution would require less die area than a comparable 2^N comparator flash converter design. This new concept proved of great value in their design, but space-saving was not its only benefit. Time interleaving of ADCs offers a conceptually simple method for multiplying the sample rate of existing high-performing ADCs, such as the 14-bit, 105-MSPS AD6645 and the 12-bit, 210-MSPS AD9430. In many different applications, this concept has been leveraged to benefit systems that require very high sample rate analog-to-digital conversion.

While the speed and resolution of standard ADC products have advanced well beyond 4 MSPS and 7 bits, time-interleaved ADC systems (for good reasons) have not advanced far beyond 8-bit resolution. Nevertheless, at 8-bit performance levels, this concept has been widely adopted in the test and measurement industry, particularly for wideband digital oscilloscopes. That it continues to make an impact in this market is evidenced by the 20-GSPS, 8-bit ADC that was recently developed by Agilent Labs (Reference 28) and adopted by the Agilent Technologies Infiniium™ oscilloscope family (Reference 29). Indeed, time-interleaved ADC systems thrive at the 8-bit level, but they continue to fall short in applications that require the combination of high resolution, wide bandwidth, and wide dynamic range.

The primary limiting factor in time-interleaved ADC systems at 12- and 14-bit levels is the requirement that the channels be matched. An 8-bit system that provides a dynamic range of 50 dB can tolerate a gain mismatch of 0.25% and a clock-skew error of 5 ps. This level of accuracy can be achieved by traditional methods, such as matching physical channel layouts, using common ADC reference voltages, prescreening devices, and active analog trimming, but at higher resolutions the requirements are much tighter. Until now devices employing more innovative matching techniques have not been commercially available.

This discussion will outline in detail the matching requirements for 12- and 14-bit time-interleaved ADC systems, discuss the idea of advanced digital post-processing techniques as an enabling technology, and introduce a device employing the most promising solution to date, Advanced Filter Bank (AFB™), from V Corp Technologies, Inc. (References 31 and 31).

Time interleaving ADC systems employ the concept of running M ADCs at a sample rate that is 1/M of the overall system sample rate. Each channel is clocked at a phase that enables the system as a whole to sample at equally spaced increments of time, creating the seamless image of a single ADC sampling at full speed. Figure 8.150 illustrates the block- and timing diagrams of a typical four-channel, time-interleaved ADC system.

Each of the four ADC channels runs at one-fourth the system's sample rate, spaced at 90° intervals. The final output data stream is created by interleaving all of the individual channel data outputs in the proper sequence (e.g., 1, 2, 3, 4, 1, 2, etc.). In a two-converter example, both ADC channels are clocked at one-half of the overall system's sample rate, and they are 180° out of phase with one another.

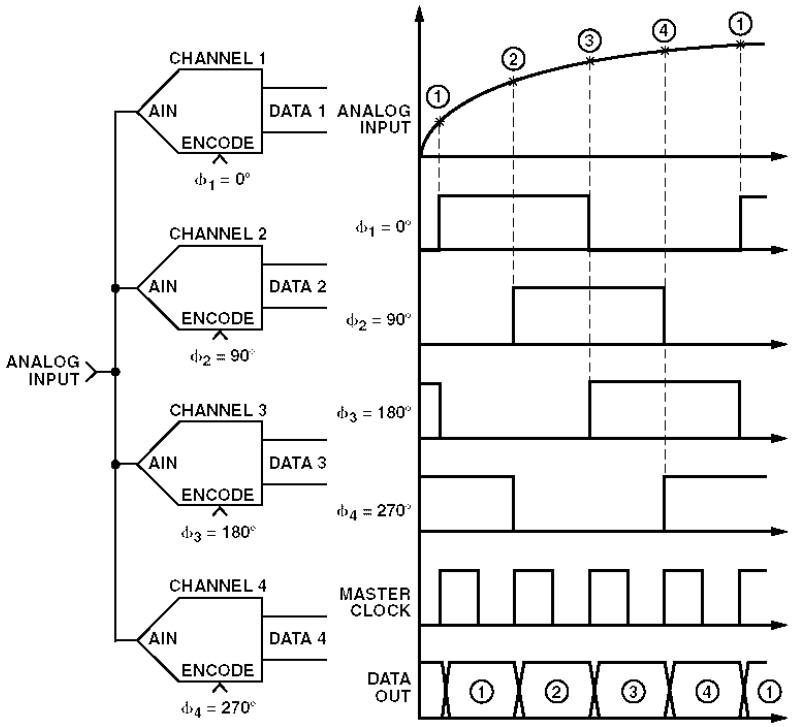


Figure 8.150: *Time-Interleaved ADCs*

For simplicity, this discussion focuses primarily on two-converter systems, but the concepts can be extended to four-converter (Reference 35). A two-converter interleaved system is shown in Figure 8.151 where two 12-bit, 200-MSPS ADCs are interleaved to produce an effective sampling rate of 400 MSPS.

As mentioned, channel-to-channel matching has a direct impact on the dynamic range performance of a time-interleaved ADC system. Mismatches between the ADC channels result in dynamic range degradation that—in an FFT plot—show up as spurious frequency components called *image spurs* and *offset spurs*. The image spur(s) associated with time-interleaved ADC systems are a direct result of gain and phase mismatches between the ADC channels. The gain and phase errors produce error functions that are orthogonal to one another. Both contribute to the image-spur energy at the same frequency location(s). The offset spur is generated by offset differences between the ADC channels. Unlike the image spur(s), the offset spurs are not dependent on the input signal. For a given offset mismatch, the offset spur(s) will always be at the same level. Extensive studies of the behavior of these spurs have resulted in several mathematical methods for characterizing the relationship between channel matching errors and dynamic range performance (References 32 and 33).

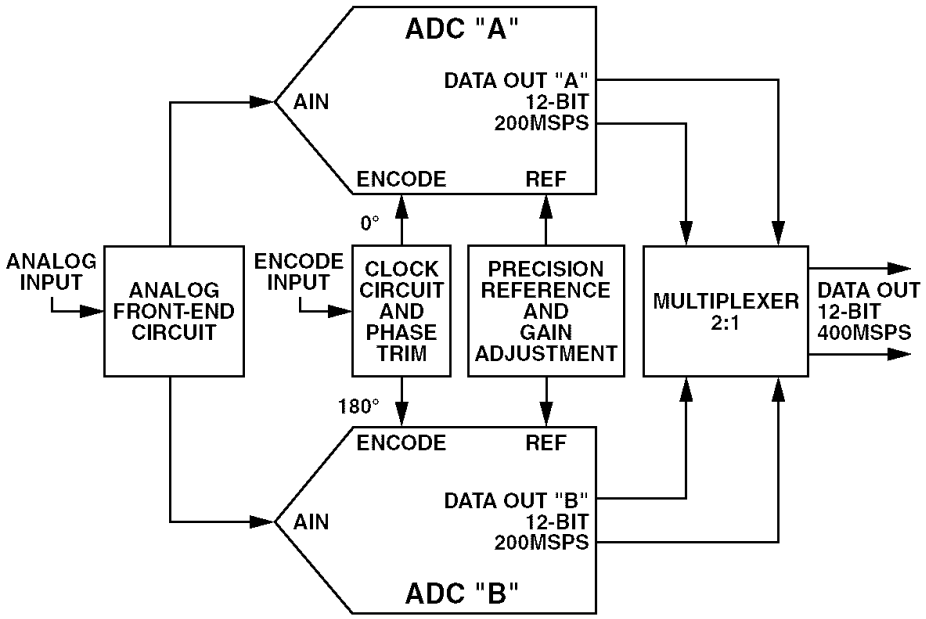


Figure 8.151: *Two-Converter Time-Interleaved 12-Bit 400-MSPS ADC*

While these methods are thorough and very useful, the "error voltage" approach used here provides a simple method for understanding the relationship without requiring a deep study of complex mathematical derivations. This approach is based on the same philosophy used in Analog Devices Application Note AN-501 (Reference 34) to establish the relationship between aperture jitter and signal-to-noise (SNR) degradation in ADCs. The error voltage is defined as the difference between the "expected" sample voltage and the "actual" sample voltage. These differences are a result of a large subset of errors that fall into three basic categories: gain, phase, and offset mismatches.

In a two-converter interleaved system, the error voltages generated by gain and phase mismatches result in an image spur that is located at Nyquist minus the analog input frequency. The offset mismatch generates an error voltage that results in an offset spur that is located at Nyquist. Since the offset spur is located at the edge of the Nyquist band, designers of two-channel systems can typically plan their system frequency around it, and focus their efforts on gain- and phase matching. Figure 8.152 displays a typical FFT plot for a two-channel system showing these errors.

In a four-converter interleaving system, there are three image spurs and two offset spurs. The image spurs, generated by gain and phase mismatches between the ADC channels, are located at (1) Nyquist minus the analog input frequency and (2) one-half Nyquist plus or minus the analog input frequency. The offset spurs are located at Nyquist and at one-half of Nyquist (middle of the band).

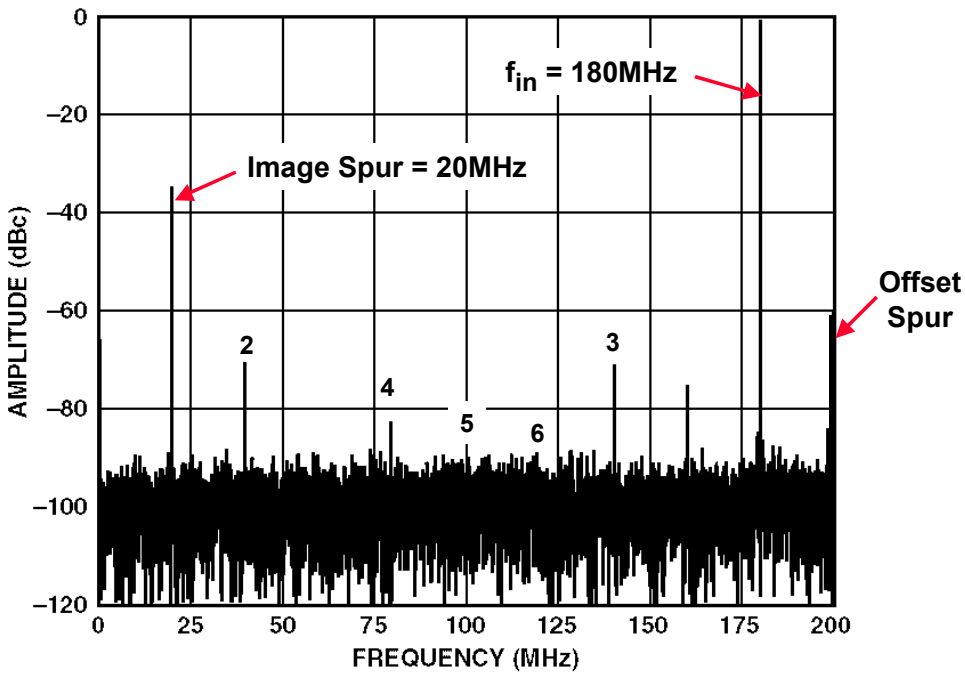


Figure 8.152: *Two-Converter Interleaved FFT Plot,*
f_s = 400 MSPS, f_{in} = 180 MHz

Once the error voltages from each of the three mismatch groups are known, the following equations can be used to calculate the image and offset spurs (IS_{gain}, IS_{phase}, IS_{total}, OS_{offset}) in a single-tone, two-converter system:

$$IS_{gain(dB)} = 20\log(IS_{gain}) = 20\log\left(\frac{G_e}{2}\right), \text{ where} \qquad \text{Eq. 8.23}$$

$$G_e = \text{gain error ratio} = \left|1 - \frac{V_{FSA}}{V_{FSB}}\right|, \qquad \text{Eq. 8.24}$$

$$IS_{phase(dB)} = 20\log(IS_{phase}) = 20\log\left(\frac{\theta_{ep}}{2}\right), \qquad \text{Eq. 8.25}$$

Where $\theta_{ep} = \omega_a \Delta t_e$ (radians)

ω_a = analog input frequency

Δt_e = clock skew error.

$$IS_{total(dB)} = 20\log\sqrt{(IS_{gain})^2 + (IS_{phase})^2} \qquad \text{Eq. 8.26}$$

$$OS_{offset(dB)} = 20\log\left(\frac{\text{Offset}}{2\times\text{Total Codes}}\right), \qquad \text{Eq. 8.27}$$

Where Offset = channel-to-channel offset (codes).

As noted earlier, the gain and phase errors generate error functions that are orthogonal (Reference 32), requiring a "root-sum-square" combination of their individual contributions to the image spur. Using these equations, an error budget can be developed to determine what level of matching will be required to maintain a given dynamic range requirement. For example, a 12-bit dynamic range requirement of 74 dBc at an input frequency of 180 MHz would require gain matching better than 0.02% and aperture delay matching better than 300 fs! If the gain can be perfectly matched, the aperture delay matching can be "relaxed" to approximately 350 fs. Figure 8.153 provides the matching requirements for several different cases to illustrate the extreme precision required to make a classical time-interleaved A/D conversion system work at 12- and 14-bit resolutions over wide bandwidths.

PERFORMANCE REQUIREMENT AT 180 MHz	SFDR (dBc)	GAIN MATCHING (%)	APERTURE TIME MATCHING (fs)
12-Bits	74	0.04	0
12-Bits	74	0	350
12-Bits	74	0.02	300
14-Bits	86	0.01	0
14-Bits	86	0	88
14-Bits	86	0.005	77

Figure 8.153: *Time-Interleaved ADC Matching Requirements*

The traditional, 2-channel time-interleaved ADC shown in Figure 8.151 achieves the first level of matching by reducing the physical and electrical differences between the channels. For example, gain matching is typically controlled by the use of common reference voltages and carefully matched physical layouts. Phase matching is achieved by manually tuning the electrical length of the clock (or analog input) paths and/or through special trimming techniques that control an electrical characteristic of the clock distribution circuit (rise/fall times, bias levels, trigger level, etc.). The offset matching depends on the offset performance of the individual ADCs.

Many of these matching approaches are based on careful analog design and trim techniques. While there has been an abundance of excellent ideas to address these tough matching requirements, many of them require additional circuits that add error sources of their own—defeating the original purpose of achieving precise gain and phase matching. An example of such an idea would be setting the rise and fall times of the two different clock signals. Any circuit that could provide this level of control would be subjected to

increased influence of power supply voltage—and temperature—on each channel's phase behavior.

Advanced Digital Post Processing

The development of new digital signal processing techniques, along with the advances in inexpensive, high-speed, configurable digital hardware platforms (DSPs, FPGAs, CPLDs, ASICs, etc.), has opened the way for breakthroughs in time-interleaving ADC performance. Digital post-processing approaches have several advantages over classical analog matching techniques. They are flexible in their implementation and can be designed for precision well beyond the ADC resolutions of interest. A conceptual view of how digital signal processing techniques can impact time-interleaved system architectures can be found in Figure 8.154.

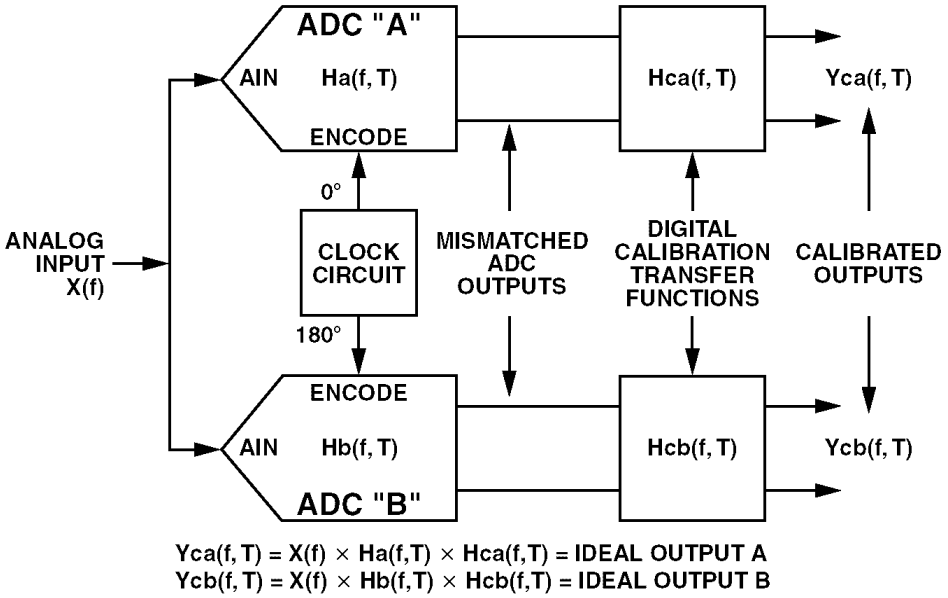


Figure 8.154: *Example of Digital Post-Processing Architecture*

This concept employs a set of digital calibration transfer functions that process each ADC's output data, creating a new set of "calibrated outputs." These digital calibration transfer functions can be implemented using a variety of digital filter configurations (FIR, IIR, etc.). They can be as simple as trimming the gain of one channel or as complicated as trimming the gain, phase, and offset of each channel over wide bandwidths and temperature ranges.

Wide bandwidth and temperature matching presents the greatest opportunity—and challenge—for using digital post-processing techniques to improve the performance of time-interleaving ADC systems. The mathematical derivations required for designing the digital calibration transfer functions for multiple ADC channels over wide bandwidths and temperature ranges are extremely complex and not readily available. However, a great deal of academic work has been invested in this area, creating a number of interesting solutions. One of these solutions, known as Advanced Filter Bank™ (AFB), stands out in its ability to provide a platform for a significant breakthrough.

Advanced Filter Bank (AFB)

AFB is one of the first commercially available digital post- processing technologies to make a significant impact on the performance of time-interleaving ADC systems. By providing precise channel-to-channel gain, phase, and offset matching over wide bandwidths and temperature ranges, AFB is well-positioned to solidly establish time-interleaving ADC systems in the area of high-speed, 12-/14-bit applications. Besides its matching functions, AFB also provides phase linearization and gain-flatness compensation for ADC systems. Figure 8.155 displays a basic block diagram representation of a system employing AFB.

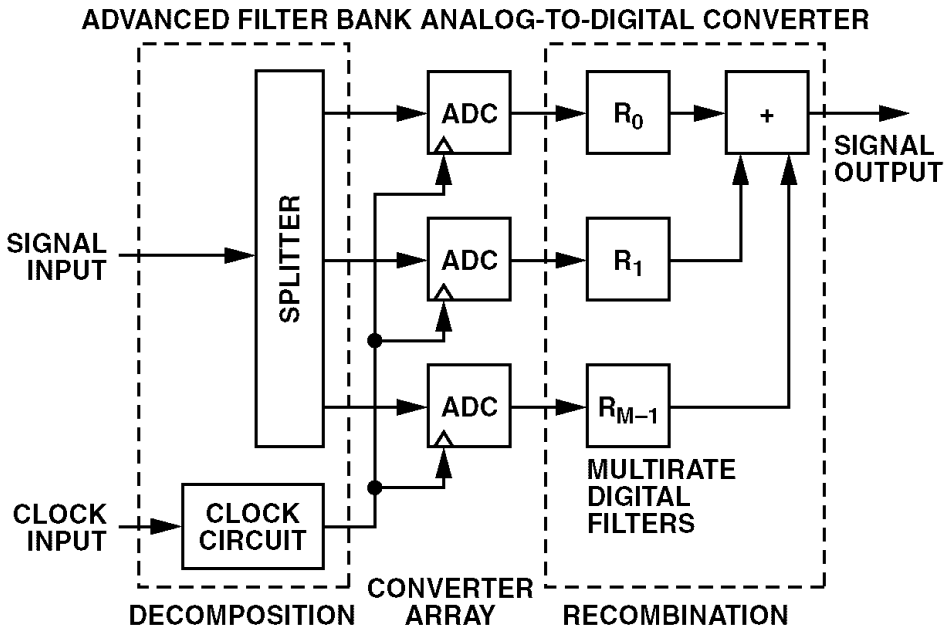


Figure 8.155: *AFB Basic Block Diagram*

By using a unique multirate FIR filter structure, AFB can be easily implemented into a convenient digital hardware platform, such as an FPGA or CPLD. The FIR coefficients are calculated using a patented method that involves starting with the equations seen in Figure 8.154, and then applying a variety of advanced mathematical techniques to solve for the digital calibration transfer function.

AFB enables time-interleaving ADC systems to use up to 90% of their Nyquist band, and can be configured to operate in any Nyquist zone of the converter (e.g., first, second, third, etc.) The appropriate Nyquist zone can be selected using a set of logic inputs, which control the required FIR coefficients.

AFB Design Example: The AD12400 12-Bit, 400-MSPS ADC

The AD12400 is the first member of a new family of Analog Devices products that leverage time interleaving and AFB. Its performance will be used to illustrate what can be achieved when state-of-the-art ADC design is combined with advanced digital post-

processing technologies. Figure 8.156 illustrates the AD12400's block diagram and its key circuit functions. The AD12400 employs a unique analog front-end circuit with 400-MHz input bandwidth, two 12-bit, 200-MSPS ADC channels, and an AFB implementation using an advanced field-programmable gate array (FPGA). It was designed using many of the classical matching techniques discussed above, together with a very low jitter clock distribution circuit. These key components are combined to develop a 12-bit, 400-MSPS ADC module that performs very well over 90% of the Nyquist band and over an 85°C temperature range. It has an analog input bandwidth of 400 MHz.

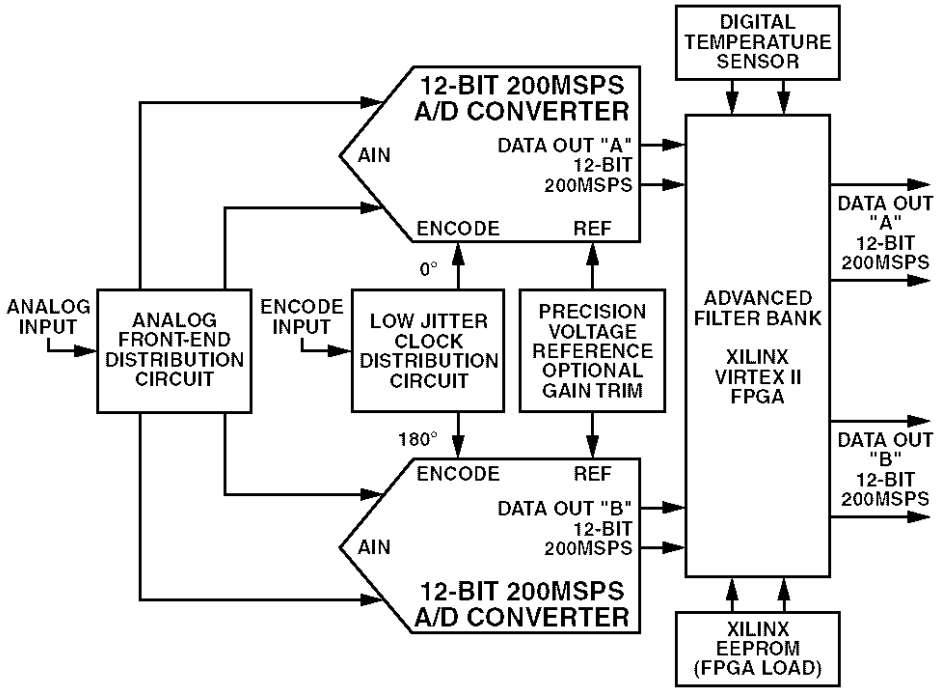


Figure 8.156: *AD12400 12-Bit, 400MSPS ADC Block Diagram*

The ADCs' transfer functions are obtained using wide-bandwidth, wide-temperature range measurements during the manufacturing process. This characterization routine feeds the ADCs' measured transfer functions directly into the AFB coefficient calculation process. Once the ADCs have been characterized, and the required FIR coefficients have been calculated, the FPGA is programmed and the product is ready for action. Wide bandwidth matching is achieved using AFB's special FIR structure and coefficient calculation process. Wide temperature performance is achieved by selecting one of the multiple FIR coefficient sets, using an on-board digital temperature sensor.

The true impact of this technology can be seen in Figure 8.157. Figure 8.157A displays the image-spur performance across the first Nyquist zone of this system. The top curve in Figure 8.157A represents the performance of a 2-channel time-interleaved system that has been carefully designed to provide optimal matching in the layout. The behavior of the image spur in this curve makes it obvious that this system was manually trimmed at an analog input frequency of 128 MHz. A similar observation of Figure 8.157B suggests a manual trim temperature at 40°C.

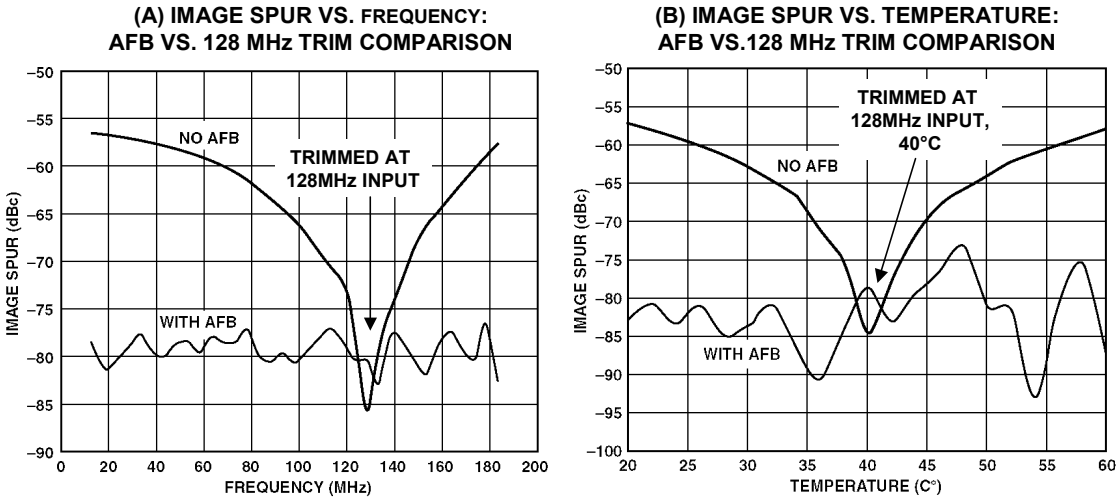


Figure 8.157: *Performance of a Manually Trimmed System "Before and After" AFB Compensation Over Frequency and Temperature Range*

Despite a careful PCB layout, tightly matched front-end circuit, tightly matched clock-distribution circuit, and common reference voltages used in the AD12400 ADC, the dynamic range degrades rapidly as the frequency and/or temperature deviates from the manual trim conditions. This rapid rate of degradation can be anticipated in any two-converter time-interleaved ADC system by analyzing some of the sensitive factors affecting this circuit. For example, the gain-temperature coefficient of a typical high-performance, 12-bit ADC is 0.02%/°C. In this case, a 10°C change in temperature would cause a 0.2% change in gain, resulting in an image spur of 60 dBc (see Equation 8.23). Considering just this single ADC temperature characteristic, the predicted image spur is 3-dB worse than the 30°C performance displayed in Figure 8.157B. By contrast, the dynamic range performance shown in these figures remains solid when the AFB compensation is enabled. In fact, the dynamic range performance surpasses the 12-bit level across a bandwidth of nearly 190 MHz and a temperature range of 40°C. Another significant advantage of this approach is that the temperature range can actually be expanded from the 20°C to 60°C range shown to 0°C to 85°C by using additional FIR coefficient sets—as embodied in the AD12400.

The AD12400 achieves impressive specifications using time interleaving followed by digital post processing. The device has a full-power input bandwidth of 300 MHz. The SNR is 64 dBFS and the SFDR is 75 dBFS for a 180-MHz input signal, sampling at 400 MSPS.

Time interleaving is growing into a significant trend in performance enhancement for high-speed ADC systems. Advanced digital post-processing methods, such as AFB, provide a convenient solution to the tough channel-matching requirements at resolution levels that were not previously achievable for time-interleaved systems. When combined with the best ADC architectures available, advanced DSP technologies, such as AFB, are ready to take high-speed ADC systems to the next level of performance and facilitate

greatly improved products and systems in demanding markets such as medical imaging, precise medicine dispensers (fluid flow measurement), synthetic aperture radar, digital beam-forming communication systems, and advanced test/measurement systems. This technology will result in many breakthroughs that will include 14-bit/400-MSPS and 12-bit/800-MSPS ADC systems in the near future.

REFERENCES:
8.6 SOFTWARE RADIO AND IF SAMPLING

1. Richard Groshong and Stephen Ruscak, "Undersampling Techniques Simplify Digital Radio," **Electronic Design**, May 23 1991, pp. 67-78.

2. Lackey and Upmall, "SPEAKeasy: The Military Software Radio," **IEEE Communications Magazine**, May 1995, pp. 56-61.

3. Brad Brannon, "Using Wide Dynamic Range Converters for Wideband Radios," **RF Design**, May 1995, pp. 50-65.

4. Jim Mitola, "The Software Radio Architecture," **IEEE Communications Magazine**, Vol. 33, No. 5, May 1995, pp. 26-38.

5. Jeffery Wepman, "Analog-to-Digital Converters and Their Applications in Radio Receivers, **IEEE Communications Magazine**, Vol. 33, No. 5, May 1995, pp. 39-45.

6. Brad Brannon, "Wide Dynamic Range A/D Converters Pave the way for Wideband Digital Radio Receivers," **EDN**, November 7, 1996, pp. 187-205.

7. Dave Robertson, "Selecting Mixed-Signal Components for Digital Communication Systems I: An Introduction, **Analog Dialogue**, 30-3, 1996, http://www.analog.com.

8. Dave Robertson, "Selecting Mixed-Signal Components for Digital Communication Systems II: Digital Modulation Schemes," **Analog Dialogue**, 30-4, 1996, http://www.analog.com.

9. Dave Robertson, "Selecting Mixed Signal Components for Digital Communication Systems III: Sharing the Channel," **Analog Dialogue**, 31-1, 1997, http://www.analog.com.

10. Dave Robertson, "Selecting Mixed Signal Component for Digital Communications Systems IV: Receiver Architecture Considerations," **Analog Dialogue**, 31-2, 1997, http://www.analog.com.

11. Dave Robertson, "Selecting Mixed-Signal Components for Digital Communications Systems V: Aliases, Images, and Spurs," **Analog Dialogue**, 31-3, 1997, http://www.analog.com.

12. Brad Brannon, "Digital Radio Receiver Design Requires Re-Evaluation of Parameters, **EDN**, November 6, 1998, pp. 163-170.

13. Brad Brannon, Dimitrios Efstathiou, and Tom Gratzek, "A Look at Software Radios: Are they Fact or Fiction?", **Electronic Design**, December 1, 1998.

14. Brad Brannon, "Designing a Superheterodyne Receiver Using an IF Sampling Diversity Chipset," **Application Note AN-502**, Analog Devices, 1998, http://www.analog.com.

15. Patrick Mannion, "Direct Conversion Prepares for Cellular Prime Time," **Electronic Design**, November 22, 1999, pp. 85-95.

16. Louis E. Frenzel, "Designers Face Tough Challenges in 3G Cellular/PCS Phone Specs," **Electronic Design**, October 2, 2000, pp. 107-122.

17. Brad Brannon and Chris Cloninger, "Redefining the Role of ADCs in Wireless," **Applied Microwave and Wireless**, March 2001, pp. 94-105.

18. Brad Brannon, "Correlating High Speed ADC Performance to Multicarrier 3G Requirements," **RF Design**, June 2003, pp. 22-28.

19. Brad Brannon, "Brad's Radio Page," http://www.converter-radio.com.

20. Brad Brannon, "Overcoming Converter Nonlinearities with Dither," **Application Note AN-410**, Analog Devices, 1995, http://www.analog.com.

21. Walt Jung, "Simple Wideband Noise Generator," Ideas for Design, **Electronic Design**, October 1, 1996.

22. Walt Jung, **Op Amp Applications**, Analog Devices, 2002, ISBN 0-916550-26-5, pp. 6.165.

23. Walt Kester, "Add Noise Dither to Blow Out ADCs' Dynamic Range," **Electronic Design, Analog Applications Supplement**, November 22, 1999, pp. 20-26.

24. Doug Mercer and Joe DiPilato, "DACs are Optimized for Communication Transmit Path," **Analog Dialogue**, 30-3, 1996, http://www.analog.com.

25. Editor, "New TxDAC Generation," **Analog Dialogue**, Volume 33- 4, April, 1999, http://www.analog.com.

26. W. C. Black Jr. and D. A. Hodges, "Time Interleaved Converter Arrays," **IEEE International Conference on Solid State Circuits**, February 1980, pp. 14-15.

27. W. C. Black Jr. and D. A. Hodges, "Time Interleaved Converter Arrays," **IEEE Journal of Solid State Circuits**, December 1980, Volume 15, pp. 1022-1029.

28. K. Poulton, et al., "A 20GS/s 8-b ADC with a 1MB Memory in 0.18 micron CMOS," **IEEE International Conference on Solid State Circuits**, February 2003, pp. 318-319, 496.

29. Press Release, "Agilent Technologies Introduces Industry First 6-GHz, 20-GSample/s-Per-Channel Oscilloscope and Probing Measurement System," Agilent Technologies Web Page, November 1, 2002, http://www.agilent.com/about/newsroom/presrel/archive.html.

30. S. Velazquez, "High-Performance Advanced Filter Bank Analog-to-Digital Converter for Universal RF Receivers," **IEEE SP International Symposium on Time-Frequency and Time-Scale Analysis**, 1998, pp. 229-232.

31. Technical Description, "Advanced Filter Bank (AFB) Analog-to-Digital Converter Technical Description," V Corp Technologies, http://www.v-corp.com/analogfilterbank.htm.

32. N. Kurosawa, et al., "Explicit Analysis of Channel Mismatch Effects in Time Interleaved ADC Systems," **IEEE Transactions on Circuits and Systems I - Fundamental Theory and Applications**, Volume 48, Number 3, March 2003.

33. M. Gustavsson, J. J. Wikner and N. N. Tan, **CMOS Data Converters for Communications**, Boston: Kluwer Academic Publishers, 2000, pp. 257-267.

34. Brad Brannon, "Aperture Uncertainty and ADC System Performance," **Application Note, AN-501**, Analog Devices, Inc., http://www.analog.com.

35. Mark Looney, "Advanced Digital Post-Processing Techniques Enhance Performance in Time-Interleaved ADC Systems," **Analog Dialogue**, 37-8, August 2003, http://www.analog.com.

NOTES:

SECTION 8.7: DIRECT DIGITAL SYNTHESIS (DDS)

Walt Kester

Introduction to DDS

A frequency synthesizer generates multiple frequencies from one or more frequency references. These devices have been used for decades, especially in communications systems. Many are based upon switching and mixing frequency outputs from a bank of crystal oscillators. Others have been based upon well understood techniques utilizing phase-locked loops (PLLs). This mature technology is illustrated in Figure 8.158. A fixed-frequency reference drives one input of the phase comparator. The other phase comparator input is driven from a divide-by-N counter which is in turn driven by a voltage-controlled-oscillator (VCO). Negative feedback forces the output of the internal loop filter to a value which makes the VCO output frequency N-times the reference frequency. The time constant of the loop is controlled by the loop filter. There are many tradeoffs in designing a PLL, such a phase noise, tuning speed, frequency resolution, etc., and there are many good references on the subject (References 1-5). Analog Devices has a complete selection of both integer and fractional-N PLLs as well as simulation software to aid the design process.

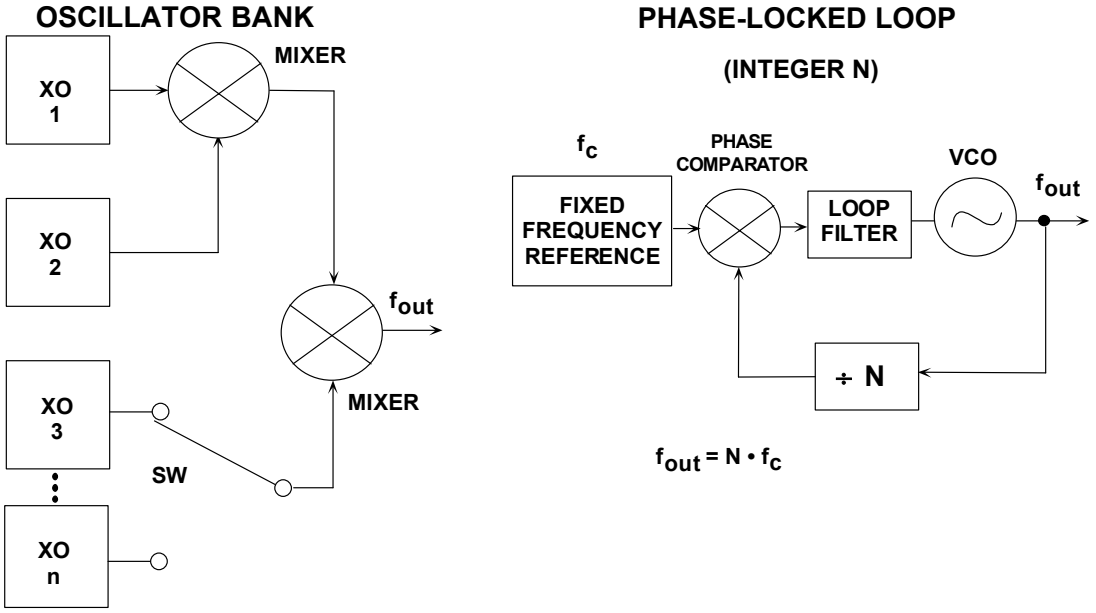


Figure 8.158: *Frequency Synthesis Using Oscillators and Phase-locked Loops*

With the widespread use of digital techniques in instrumentation and communications systems, a digitally-controlled method of generating multiple frequencies from a reference frequency source has evolved called Direct Digital Synthesis (DDS). The basic architecture is shown in Figure 8.159. In this simplified model, a stable clock drives a programmable-read-only-memory (PROM) which stores one or more integral number of

cycles of a sinewave (or other arbitrary waveform, for that matter). As the address counter steps through each memory location, the corresponding digital amplitude of the signal at each location drives a DAC which in turn generates the analog output signal. The spectral purity of the final analog output signal is determined primarily by the DAC. The phase noise is basically that of the reference clock.

The DDS system differs from the PLL in several ways. Because a DDS system is a sampled data system, all the issues involved in sampling must be considered: quantization noise, aliasing, filtering, etc. For instance, the higher order harmonics of the DAC output frequencies fold back into the Nyquist bandwidth, making them unfilterable, whereas, the higher order harmonics of the output of PLL-based synthesizers can be filtered. There are other considerations which will be discussed shortly.

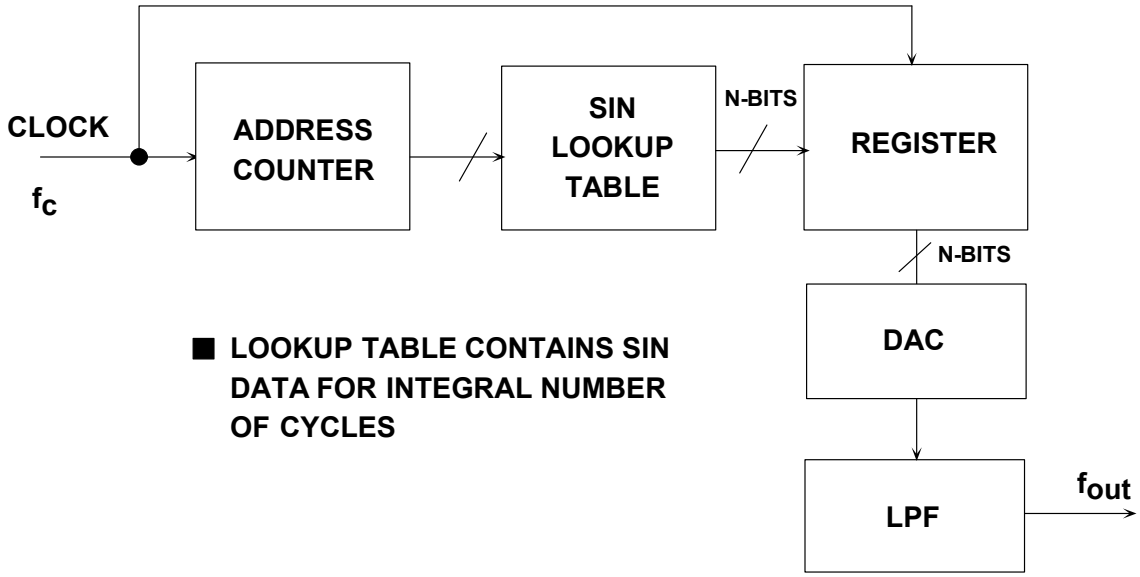


Figure 8.159: *Fundamental Direct Digital Synthesis System*

A fundamental problem with this simple DDS system is that the final output frequency can be changed only by changing the reference clock frequency or by reprogramming the PROM—making it rather inflexible. A practical DDS system implements this basic function in a much more flexible and efficient manner using digital hardware called a Numerically Controlled Oscillator (NCO). A block diagram of such a system is shown in Figure 8.160.

The heart of the system is the *phase accumulator* whose contents is updated once each clock cycle. Each time the phase accumulator is updated, the digital number, M, stored in the *delta phase register* is added to the number in the phase accumulator register. Assume that the number in the delta phase register is 00...01 and that the initial contents of the phase accumulator is 00...00. The phase accumulator is updated by 00...01 on each clock cycle. If the accumulator is 32-bits wide, 2^{32} clock cycles (over 4 billion) are required before the phase accumulator returns to 00...00, and the cycle repeats.

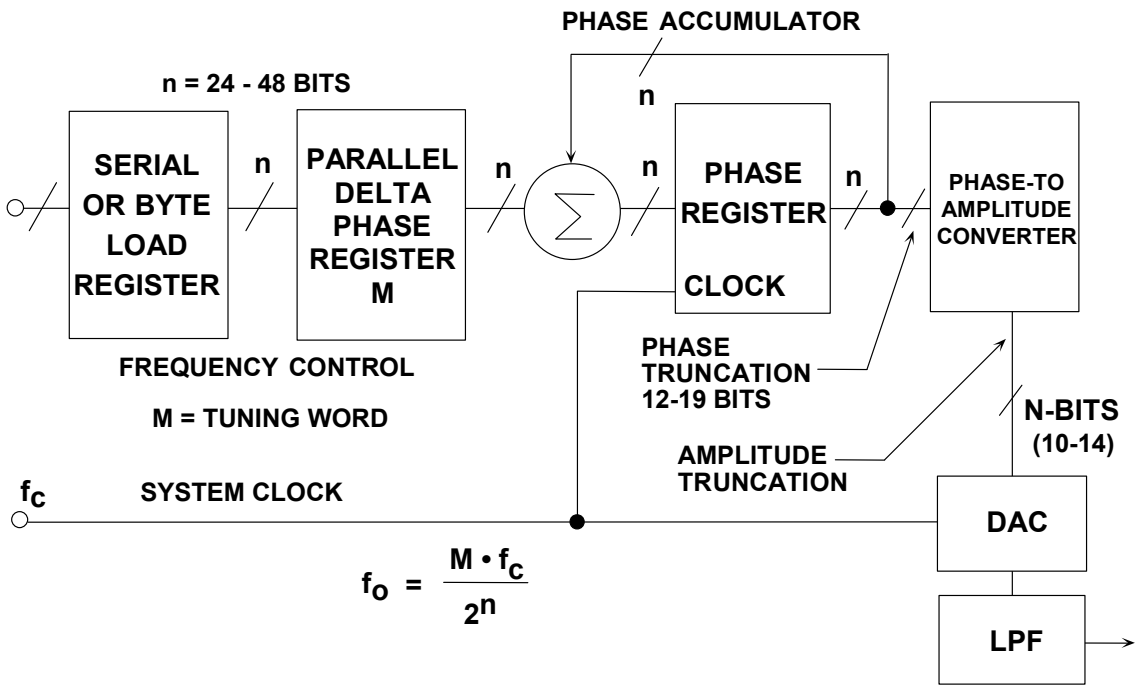


Figure 8.160: *A Flexible DDS System*

The truncated output of the phase accumulator serves as the address to a sine (or cosine) lookup table. Each address in the lookup table corresponds to a phase point on the sinewave from 0° to 360°. The lookup table contains the corresponding digital amplitude information for one complete cycle of a sinewave. The lookup table therefore maps the phase information from the phase accumulator into a digital amplitude word, which in turn drives the DAC. In practice, only data for 90° is required because the quadrature data is contained in the two MSBs. In order to further reduce the size of the lookup tables, various proprietary algorithms have been developed to compute the sine values, however the fundamental concept is still the same.

Consider the case for n = 32, and M = 1. The phase accumulator steps through each of 2^{32} possible outputs before it overflows. The corresponding output sinewave frequency is equal to the clock frequency divided by 2^{32}. If M = 2, then the phase accumulator register "rolls over" twice as fast, and the output frequency is doubled. This can be generalized as follows.

For an n-bit phase accumulator (n generally ranges from 24 to 32 in most DDS systems), there are 2^n possible phase points. The digital word in the delta phase register, M, represents the amount the phase accumulator is incremented each clock cycle. If f_c is the clock frequency, then the frequency of the output sinewave is equal to:

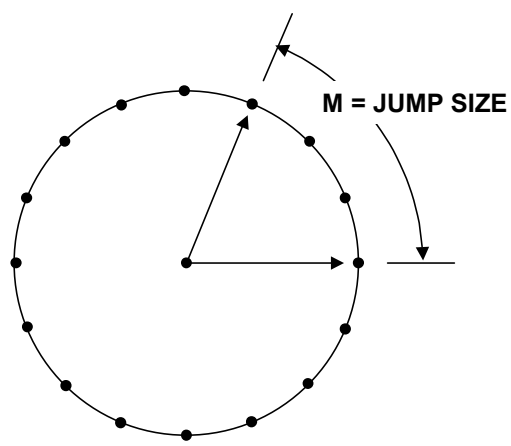
$$f_o = \frac{M \cdot f_c}{2^n}. \qquad \text{Eq. 8.28}$$

This equation is known as the DDS "tuning equation." Note that the frequency resolution of the system is equal to $f_c/2^n$. For n = 32, the resolution is greater than one part in four

billion! In a practical DDS system, all the bits out of the phase accumulator are not passed on to the lookup table, but are truncated, thereby reducing the size of the lookup table without affecting frequency resolution. The amount of truncation depends upon the resolution and performance of the output DAC. In general, the phase address information should have 2 to 4 bits more resolution than the DAC, but this can vary some from product to product. The objective is to use enough resolution in the lookup table address so that the overall noise and distortion of the analog output signal is limited by the DAC and not the effects of phase truncation.

The basic DDS system described above is extremely flexible and has high resolution. The frequency can be changed instantaneously with no phase discontinuity by simply changing the contents of the M-register. However, practical DDS systems first require the execution of a serial, or byte-loading sequence to get the new frequency word into an internal buffer register which precedes the parallel-output M-register. This is done to minimize package pin count. After the new word is loaded into the buffer register, the parallel-output delta phase register is clocked, thereby changing all the bits simultaneously. The number of clock cycles required to load the delta-phase buffer register determines the maximum rate at which the output frequency can be changed.

Figure 8.161 shows another way to view the operation of the phase accumulator. The sine wave oscillation is visualized as a vector rotating around a phase circle. Each designated point on the phase wheel corresponds to the equivalent point on a cycle of a sine waveform. As the vector rotates around the wheel, a corresponding output sinewave is being generated. One revolution of the vector around the phase wheel, at constant speed, results in one complete cycle of the output sinewave. The phase accumulator is utilized to provide the equivalent of the vector's linear rotation around the phase wheel. The contents of the phase accumulator corresponds to the points on the cycle of the output sinewave.



$$f_O = \frac{M \cdot f_C}{2^n}$$

n	Number of Points = 2^n
8	256
12	4,096
16	65,536
20	1,048,576
24	16,777,216
28	268,435,456
32	4,294,967,296
48	281,474,976,710,656

Figure 8.161: *Digital Phase Wheel*

The number of discrete points on the phase circle is determined by the resolution of the phase accumulator. For an n-bit accumulator, there are 2^n number of points on the phase circle. The digital word in the delta phase register (M) represents the "jump size" between updates. It commands the phase accumulator to jump by M points on the phase circle each time the system is clocked.

Figure 8.162 shows the signal flow through the DDS architecture. The phase accumulator is actually a modulus M counter that increments its stored number each time it receives a clock pulse. The magnitude of the increment is determined by the binary input number or word (M) contained in the delta phase register that is summed with the overflow of the counter. The digital phase information from the phase accumulator is converted into a corresponding digital amplitude by the phase-to-amplitude converter. Finally, the DAC converts the digital amplitude into a corresponding analog signal.

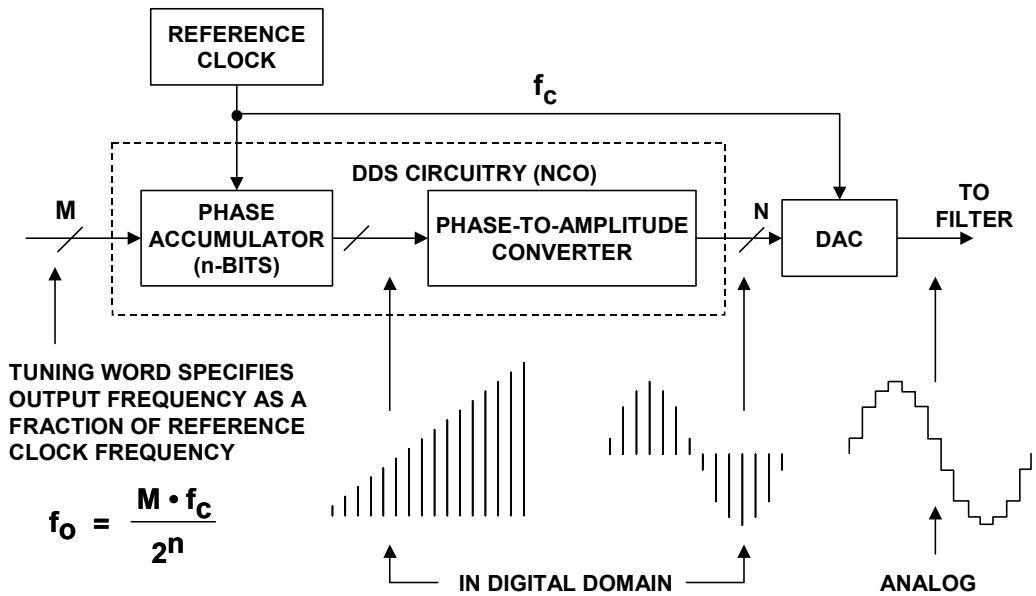


Figure 8.162: *Signal Flow Through the DDS Architecture*

When IC DDS systems became popular in the mid 1980s, the digital NCO was generally fabricated on a CMOS process, and the DAC on a bipolar process, thereby yielding a two-chip solution. Today, however, modern CMOS processes are suitable for not only the digital circuits but for the high performance DAC as well (as illustrated by the many TxDACs currently offered by Analog Devices). Modern DDS systems therefore are fully integrated and include many additional options as well.

Aliasing in DDS Systems

There is one important limitation to the range of output frequencies that can be generated from the simple DDS system. The Nyquist Criteria states that the clock frequency (sample rate) must be at least twice the output frequency. Practical limitations restrict the actual highest output frequency to about 40% of the clock frequency. Figure 8.163 shows the output of a DAC in a DDS system where the output frequency is 30 MHz and the clock frequency is 100 MSPS. An anti-imaging filter must follow the reconstruction DAC to remove the lower image frequency (100 – 30 = 70 MHz) as shown in the figure.

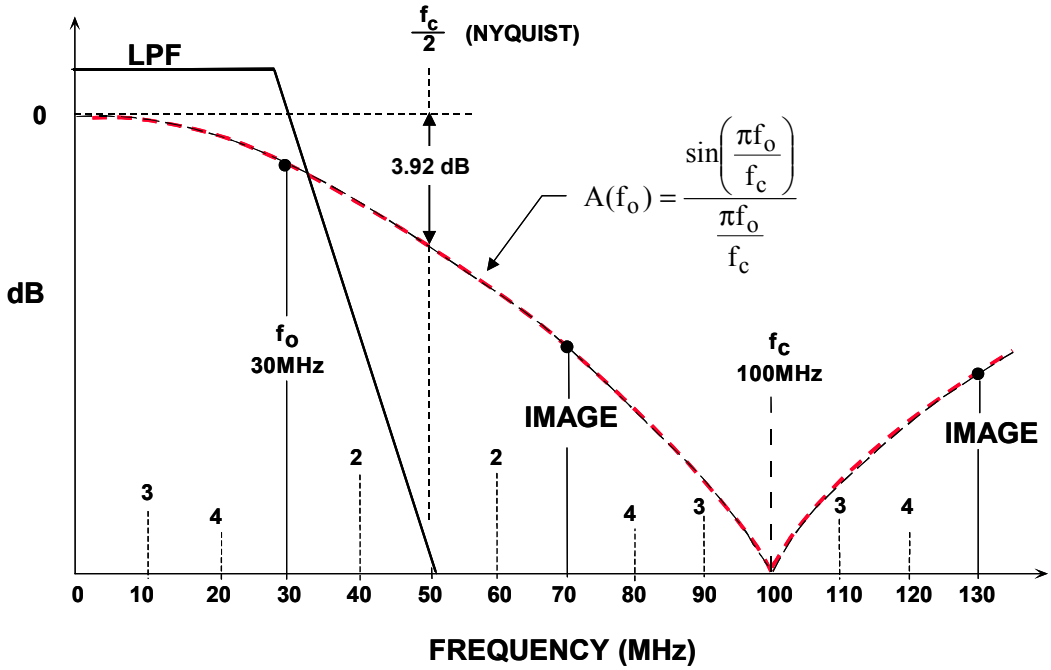


Figure 8.163: *Aliasing in a DDS System Clocked at 100 MSPS with a 30-MHz Output*

Note that the amplitude response of the DAC output (before filtering) follows a sin(x)/x response with zeros at the clock frequency and multiples thereof. The exact equation for the normalized output amplitude, $A(f_o)$, is given by:

$$A(f_o) = \frac{\sin\left(\frac{\pi f_o}{f_c}\right)}{\frac{\pi f_o}{f_c}}, \qquad \text{Eq. 8.29}$$

where f_o is the output frequency and f_c is the clock frequency.

This rolloff occurs because the DAC output is not a series of zero-width impulses (as in a perfect impulse re-sampler), but a series of rectangular pulses whose width is equal to the reciprocal of the update rate. The amplitude of the sin(x)/x response is down 3.92 dB at the Nyquist frequency (1/2 the DAC update rate). In practice, the transfer function of the antialiasing filter is designed to compensate for the sin(x)/x rolloff so that the overall frequency response is relatively flat up to the maximum output DAC frequency (generally 40% of the update rate).

Another important consideration is that unlike a PLL-based system, the higher order harmonics of the fundamental output frequency in a DDS system will fold back into the baseband because of aliasing. These harmonics cannot be removed by the antialiasing

filter. For instance, if the clock frequency is 100 MSPS, and the output frequency is 30 MHz, the second harmonic of the 30-MHz output signal appears at 60 MHz (out of band), but also at 100 – 60 = 40 MHz (an inband aliased component). Similarly, the third harmonic (90 MHz) appears inband at 100 – 90 = 10 MHz, and the fourth at 120 –100 = 20 MHz. Higher order harmonics also fall within the Nyquist bandwidth (dc to $f_C/2$). The locations of the first four harmonics are labeled in the diagram.

Frequency Planning in DDS Systems

In many DDS applications, the spectral purity of the DAC output is of primary concern. Unfortunately, the measurement, prediction, and analysis of this performance is complicated by a number of interacting factors.

It is wise to carefully choose the output frequency and the clock frequency such that the aliased harmonics discussed above do not fall close to the fundamental output frequency, and can therefore be removed with a bandpass filter.

Even an ideal N-bit DAC can produce unwanted harmonics in a DDS system. The amplitude of these harmonics is highly dependent upon the ratio of the output frequency to the clock frequency. This is because the spectral content of the DAC quantization noise varies as this ratio varies, even though its theoretical rms value remains equal to $q/\sqrt{12}$ (where q is the weight of the LSB). The assumption that the quantization noise appears as white noise and is spread uniformly over the Nyquist bandwidth is simply not true in a DDS system (it is more apt to be a true assumption in an ADC-based system, because the ADC adds a certain amount of noise to the signal which tends to "dither" or randomize the quantization error. However, a certain amount of correlation still exists). For instance, if the DAC output frequency is set to an exact submultiple of the clock frequency, then the quantization noise will be concentrated at multiples of the output frequency, i.e., it is highly signal dependent. If the output frequency is slightly offset, however, the quantization noise will become more random, thereby giving an improvement in the effective SFDR.

This is illustrated in Figure 8.164, where a 4096 point FFT is calculated based on digitally generated data from an ideal 12-bit DAC. In the left-hand diagram, the ratio between the clock frequency and the output frequency was chosen to be exactly 32 (128 cycles of the sinewave in the FFT record length), yielding an SFDR of about 78 dBc. In the right-hand diagram, the ratio was changed to 32.25196850394 (127 cycles of the sinewave within the FFT record length), and the effective SFDR is now increased to 92 dBc. In this ideal case, we observed a change in SFDR of 16 dB just by slightly changing the frequency ratio.

Best SFDR can therefore be obtained by the careful selection of the clock and output frequencies. However, in some applications, this may not be possible. In ADC-based systems, adding a small amount of random noise to the input tends to randomize the quantization errors and reduce this effect. The same thing can be done in a DDS system as shown in Figure 8.165 (Reference 16). The pseudo-random digital noise generator output is added to the DDS sine amplitude word before being loaded into the DAC. The amplitude of the digital noise is set to about ½ LSB. This accomplishes the randomization

process at the expense of a slight increase in the overall output noise floor. In most DDS applications, however, there is enough flexibility in selecting the various frequency ratios so that this type of dithering is not required.

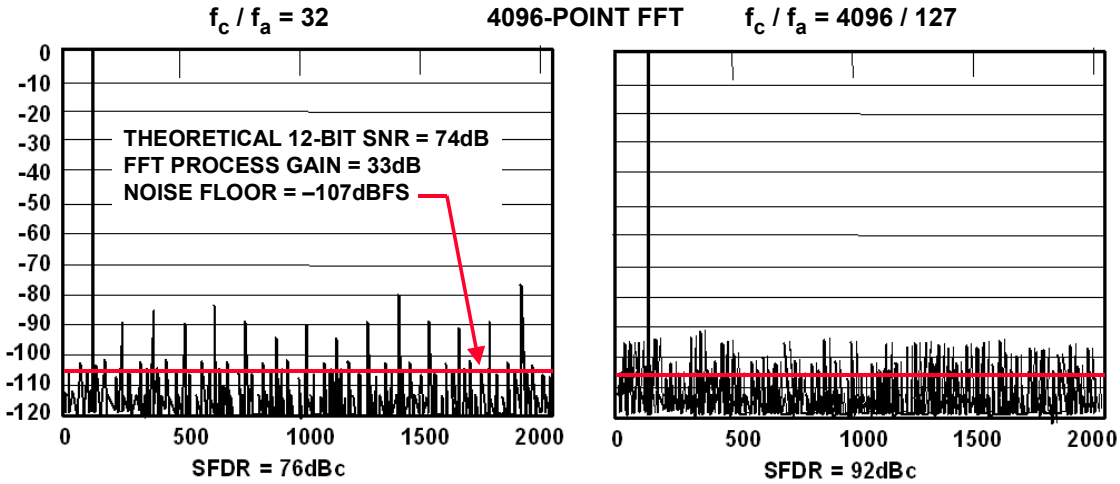


Figure 8.164: *Effect of Ratio of Sampling Clock to Output Frequency on SFDR for Ideal 12-bit DAC*

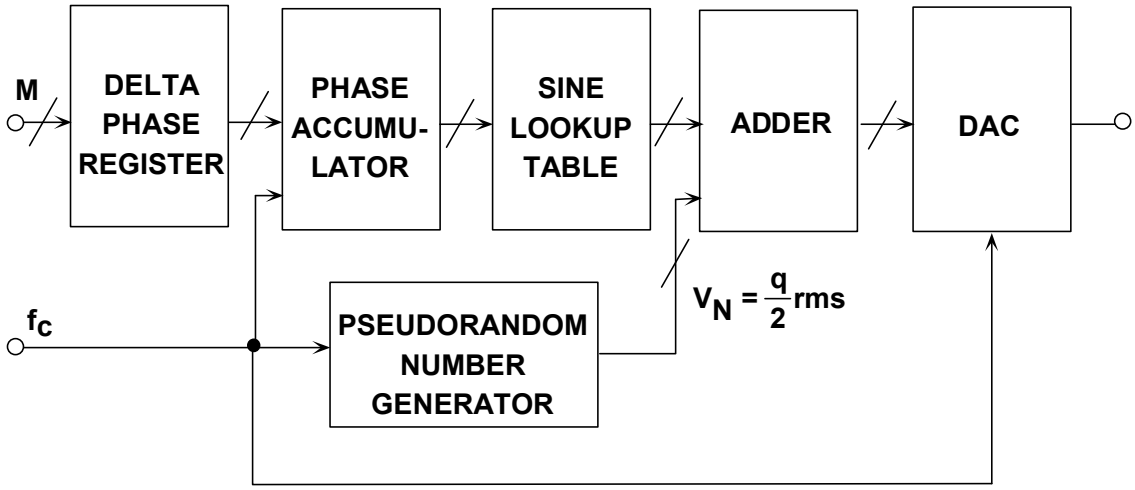


Figure 8.165: *Injection of Digital Dither in a DDS System to Randomize Quantization Noise and Increase SFDR*

Modern Integrated DDS Systems

DDS integrated circuits have proliferated in the last several years, and there are a large number of devices to choose from. In this section we will highlight some typical DDSs which offer a high level of integration and flexibility.

The AD9834 is a member of Analog Devices' low power family of DDS parts. It operates up to 50 MSPS and dissipates only 20 mW. A simplified functional diagram is shown in Figure 8.166, and key specifications are highlighted in Figure 8.167.

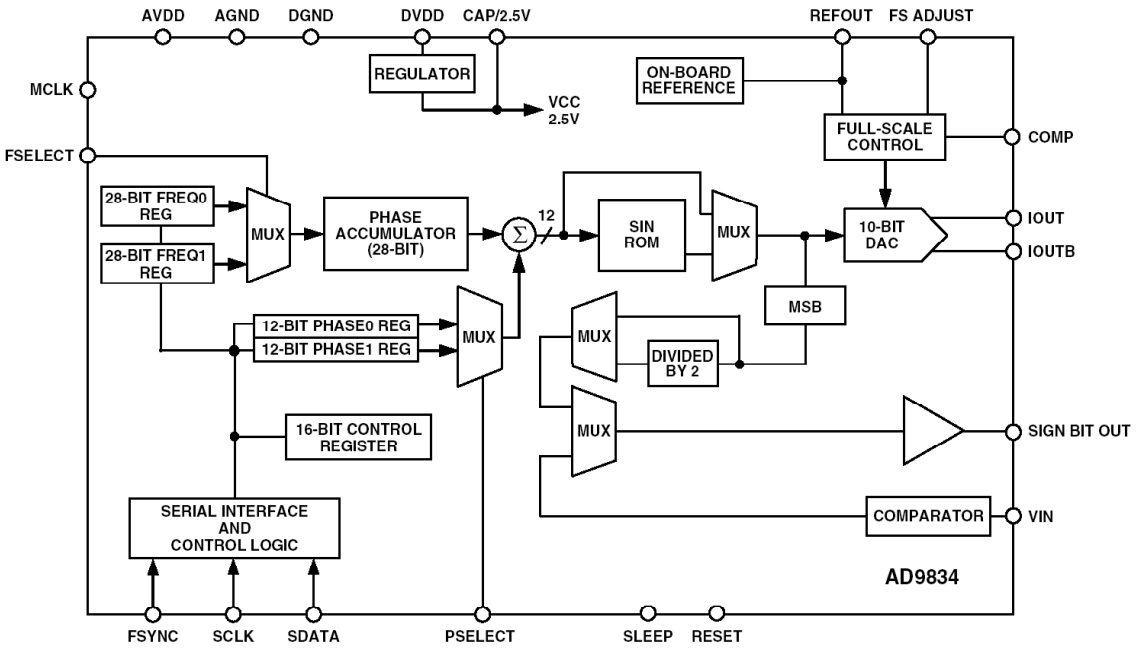


Figure 8.166: *AD9834 Low Power (20mW), 50-MSPS DDS Synthesizer*

- **Sinusoidal/Triangular DAC Output**
- **Programmable phase and frequency**
- **Narrow-Band SFDR >72 dB**
- **10-Bit DAC, 28-Bit Phase Accumulator**
- **2.3 V to 5.5 V Operation**
  - **Low Power (20-35 mW)**
  - **Power-Down Option**
- **Two Frequency Registers and Two Phase Registers**
- **Low Jitter Clock Output**
- **Narrow Band SFDR >72 dB**
- **40 Mhz SPI Serial Interface**
- **25 MHz (AD9833) / 50 MHz (AD9834) Speed**
- **Serial Loading**
- **Extended Temperature Range: –40°C to +105°C**
- **10-Lead µSOIC (AD9833) or 20-Lead TSSOP (AD9834)**

Figure 8.167: *AD9833/AD9834 Key Features*

The 50-MSPS AD9834 contains a 10-bit TxDAC core which yields a narrowband SFDR greater than 72 dB. The sin ROM can be bypassed to produce a triangular waveform output. The phase accumulator is 28-bits wide, and the output is truncated to 12-bits at the sin ROM lookup table address input. An on-chip comparator allows a square wave output to be produced for clock generation. The AD9834 is written to via a 3-wire serial

interface which can operate at clock rates up to 40 MHz and is compatible with DSP and microcontroller standards.

The AD9834 has a power-down pin that allows external control of the power-down mode. Sections of the device that are not being used can be powered down to minimize the current consumption.

Phase and frequency modulation capability is provided. The Frequency registers are 28-bits wide, and the phase registers are 12-bits wide. Because of the various output options available from the part, the AD9834 can be configured to suit a wide variety of applications. One of the areas where the AD9834 is suitable is in modulation applications. The part can be used to perform simple modulation such as FSK. More complex modulation schemes such as GMSK and QPSK can also be implemented using the AD9834. In an FSK application, the two frequency registers of the AD9834 are loaded with different values. One frequency will represent the space frequency, while the other will represent the mark frequency. The digital data stream is fed to the FSELECT pin, which will cause the AD9834 to modulate the carrier frequency between the two values. The AD9834 has two phase registers; this enables the part to perform PSK. With phase shift keying, the carrier frequency is phase shifted, the phase being altered by an amount that is related to the bit stream being input to the modulator. The AD9834 is also suitable for signal generator applications. With its low current consumption, the part is suitable for applications in which it can be used as a local oscillator.

Figure 8.168 summarizes the current low power DDS offerings from Analog Devices.

Parameter	AD9830	AD9831	AD9832	AD9833	AD9834	AD9835
Master Clock	50 MHz	25 MHz	25 MHz	25 MHz	50 MHz	50 MHz
DAC Resolution	10-bit	10-bit	10-bit	10-bit	10-bit	10-bit
Interface	Par	Par	Serial	Serial	Serial	Serial
Freq/Phase Registers	4 Phase, 2 Freq	4 Phase, 2 Freq	4 Phase, 2 Freq	2 Phase, 2 Freq	2 Phase, 2 Freq	4 Phase, 2 Freq
Supply Voltage	5V±5%	2.97V to 5.5V	2.97V to 5.5V	2.5V to 5.5V	2.5V to 5.5V	5V±5%
Power	275mW max	45mW max	45mW max	21mW	24mW	200mW max
Package	48-TQFP	48-TQFP	16-TSSOP	10-μSOIC	20-TSSOP	16-TSSOP
Comparator Output					Yes	

Figure 8.168: *AD983x Low Power DDS Synthesizers*

The AD9858 is a direct digital synthesizer (DDS) featuring a 10-bit DAC operating up to 1 GSPS. The AD9858 uses advanced DDS technology, coupled with an internal high speed, high performance DAC to form a digitally programmable, complete high frequency synthesizer capable of generating a frequency-agile analog output sinewave at

up to 400+ MHz. The AD9858 is designed to provide fast frequency hopping and fine tuning resolution (32-bit frequency tuning word). The frequency tuning and control words are loaded into the AD9858 via parallel (8-bit) or serial loading formats. The AD9858 contains an integrated charge pump (CP) and phase frequency detector (PFD) for synthesis applications requiring the combination of a high speed DDS along with phase-locked loop (PLL) functions. An analog mixer is also provided on-chip for applications requiring the combination of a DDS, PLL, and mixer, such as frequency translation loops, tuners, and so on. The mixer can operate at frequencies up to 2 GHz.

The AD9858 also features a divide-by-two on the clock input, allowing the external clock to be as high as 2 GHz. The AD9858 is specified to operate over the extended industrial temperature range of –40°C to +85°C. A functional block diagram is shown in Figure 8.169, and key specifications are summarized in Figure 8.170.

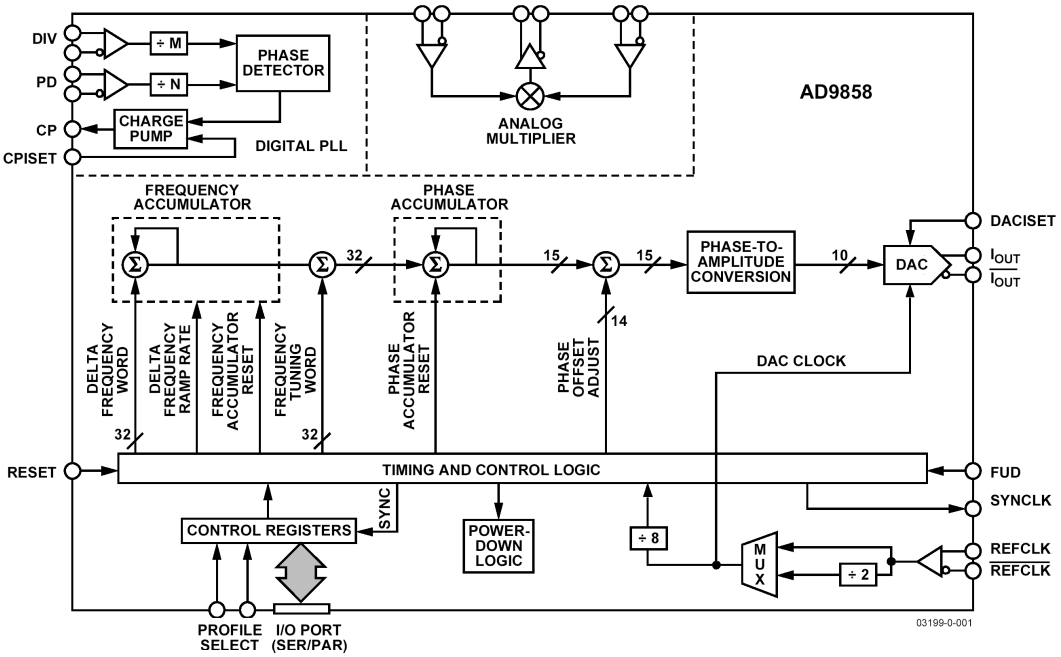


Figure 8.169: *AD9858 1-GSPS DDS with Phase Detector and Analog Multiplier*

Writing data to the on-chip digital registers that control all operations of the device easily configures the AD9858. The AD9858 offers a choice of both serial and parallel ports for controlling the device. There are four user profiles that can be selected by a pair of external pins. These profiles allow independent setting of the frequency tuning word and the phase offset adjustment word for each of four selectable configurations. The AD9858 can be programmed to operate in single-tone mode or in a frequency-sweeping mode. To save on power consumption, there is also a programmable full-sleep mode, during which most of the device is powered down to reduce current flow.

- 1 GSPS Internal Clock Speed
- Integrated 10-Bit D/A Converter
- Phase Noise <130 dBc/Hz @ 1 kHz Offset (DAC Output)
- 32-Bit Programmable Frequency Register
- Simplified 8-Bit Parallel and SPI Serial Control Interface
- Automatic Frequency Sweeping Capability
- 3.3 V Power Supply
- Power Dissipation < 2 Watts @ 1 GHz
- 100-Lead LQFP Surface-Mount Package
- Integrated Programable Charge Pump and Phase/Frequency Detector with Fast Lock Circuit
- Integrated 2 GHz Mixer

Figure 8.170: *AD9858 1-GSPS DDS Key Specifications*

Figure 8.171 shows the AD9858 configured as an upconverter using the internal phase detector and charge pump along with external filtering and a VCO to form a high-speed PLL. The basic AD9858 DDS can generate a frequency up to 400 MHz. The PLL circuitry in conjunction with a high frequency VCO and divider is capable of multiplying the reference frequency well up into the GHz region. The reference frequency into the phase detector can be as high as 150 MHz. Further details on using DDS devices as upconverters can be found in References 10, 11, and 15.

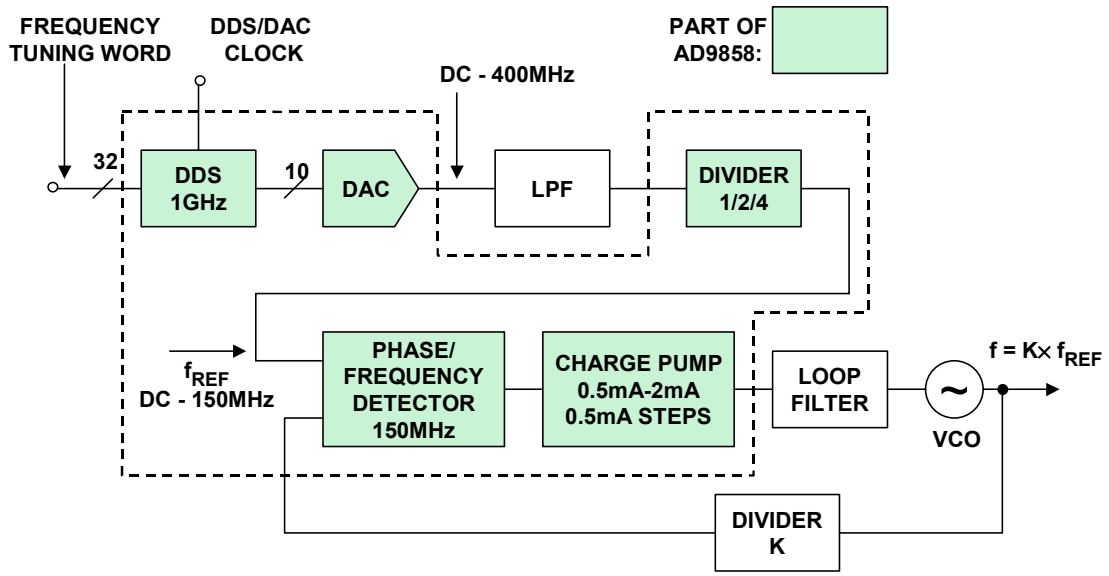


Figure 8.171: *DDS Single Loop Upconversion Using the AD9858*

Figure 8.172 summarizes the high-speed DDS products currently available from Analog Devices.

Parameter	AD9850	AD9851	AD9852	AD9854	AD9857	AD9858
Master Clock	125 MHz	180 MHz	300 MHz	300 MHz	200 MHz	1 GHz
DAC Resolution	10-bit	10-bit	12-bit	12-bit	14-bit	10-bit
Control Interface	Par / Serial	Par / Serial	Par / Serial	Par / Serial	Serial	Par/Serial
SFDR	>50 dBc @ 40 MHz Aout	>43 dBc @ 70 MHz Aout	80 dBc @ 100 MHz (±1 MHz) Aout	80 dBc @ 100 MHz (±1 MHz) Aout	80 dBc @ 65 MHz(±100 kHz) Aout	>50 dBc @ 360 MHz Aout
Supply Voltage	+3.3 V or +5.25 V	+2.7 V to +5.25 V	3.3 V	3.3 V	3.3 V	3.3 V
Power	155 mW @ 110MHz (+3.3V)	555 mW @ 180MHz	1.9 to 2.7 W	1.9 to 3.4 W	1 to 2 W	1.9W @ 1 GHz
Package	28-SSOP	28-SSOP	80-LQFP	80-LQFP	80-LQFP	100-EPAD TQFP
On-Chip Comparator	Yes	Yes	Yes	Yes	No	No
Notes		Clock-multiplier (6X)	Auto Freq. Sweep Clock multiplier (4-20X)	Quadrature Outputs	Modulator or Single Tone Mode	Auto Freq. Sweep, PLL, Mixer, 2 GHz input clocking

Figure 8.172: *AD985x High Speed DDS Synthesizers*

The AD9954 is a 400-MSPS 14-bit, 1.8-V DDS with advanced on-chip FSK modulation capability. The AD9954 is a digitally programmable, complete high frequency synthesizer capable of generating a frequency-agile analog output sinusoidal waveform at up to 200 MHz. The AD9954 is designed to provide fast frequency hopping and fine tuning resolution (32-bit frequency tuning word). The frequency tuning and control words are loaded into the AD9954 via a serial I/O port.

The AD9954 includes an integrated 1024 word × 32 bit static RAM to support flexible frequency sweep capability in several modes. The AD9954 also supports a user-defined linear sweep mode of operation. The device includes an on-chip high speed comparator for applications requiring a square wave output. The AD9954 is specified to operate over the extended industrial temperature range of –40° to +85°C. A simplified functional diagram of the AD9954 is shown in Figure 8.173, and key specifications are given in Figure 8.174. A summary of the 400-MSPS DDS parts from Analog Devices is given in Figure 8.175.

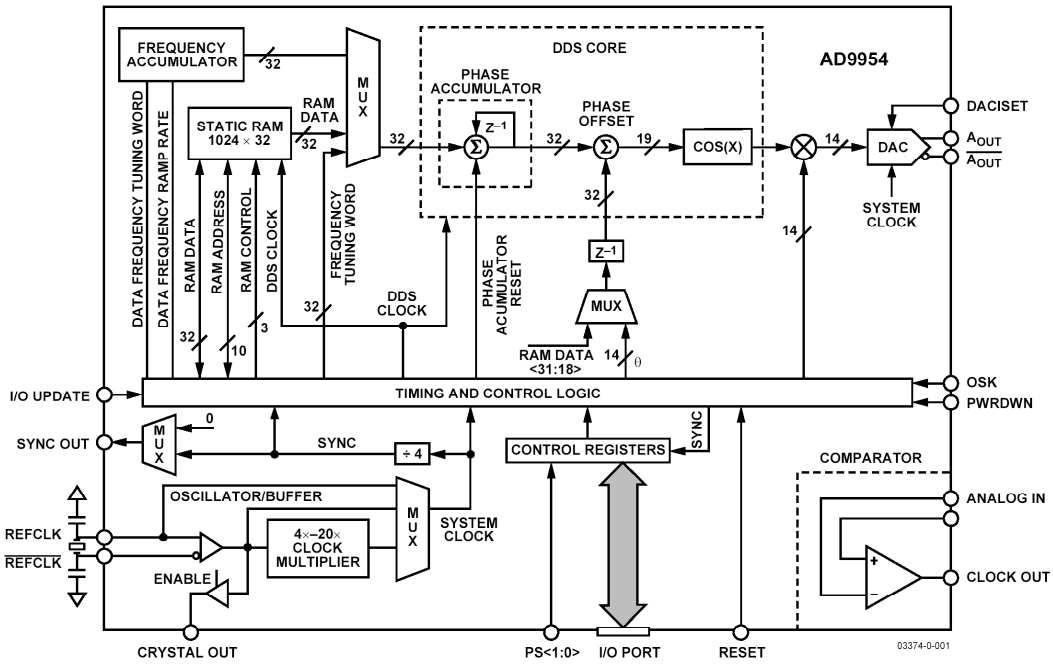


Figure 8.173: *AD9954 Low Power 400-MSPS 14-Bit Advanced FSK Modulator w/ Comparator*

- **400 MSPS Internal Clock Speed**
- **1.8 V Power Supply Operation**
- **Integrated 14-Bit DAC**
- **RAM: 1024 Word, 32-Bit**
- **14-Bit Amplitude Modulation**
- **32-Bit Programmable Frequency Register**
- **On-chip Oscillator/Buffer**
- **4× - 20× Programmable Reference Clock Multiplier**
- **High-Speed Comparator**
- **SPI Serial Control Interface**
- **Automatic Frequency Sweeping**
- **Power Dissipation < 250 mW @ 400 MSPS**
- **Small 48-lead TQFP Packaging**

Figure 8.174: *AD9954 Low Power 400-MSPS 14-Bit Advanced FSK Modulator Key Specifications*

Parameter	AD9859	AD9951	AD9952	AD9953	AD9954
Master Clock (Max)	400 MHz	400 MHz	400 MHz	400 MHz	400 MHz
DAC Resolution	10-bit	14-bit	14-bit	14-bit	14-bit
Interface	Serial	Serial	Serial	Serial	Serial
Supply Voltage	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V
Power	<250 mW	<250 mW	<250 mW	<250 mW	<250 mW
Phase, Frequency RAM				✓	✓
Automatic Frequency Sweep					✓
Comparator			✓		✓

Figure 8.175: *400-MSPS Low Power DDS Product Family*

With the availability of high performance low power CMOS processes, digital quadrature modulation capability can be added to the basic DDS function. Figure 8.176 shows a simplified block diagram of the AD9857 200-MSPS 14-bit quadrature digital upconverter. The AD9857 is intended to function as a universal I/Q modulator and agile upconverter, single-tone DDS, or interpolating DAC for communications applications. The device has excellent dynamic performance with 80-dB narrowband SFDR at a 65-MHz output frequency. Figure 8.177 summarizes Analog Devices' DDS parts which are optimized as I/Q modulators.

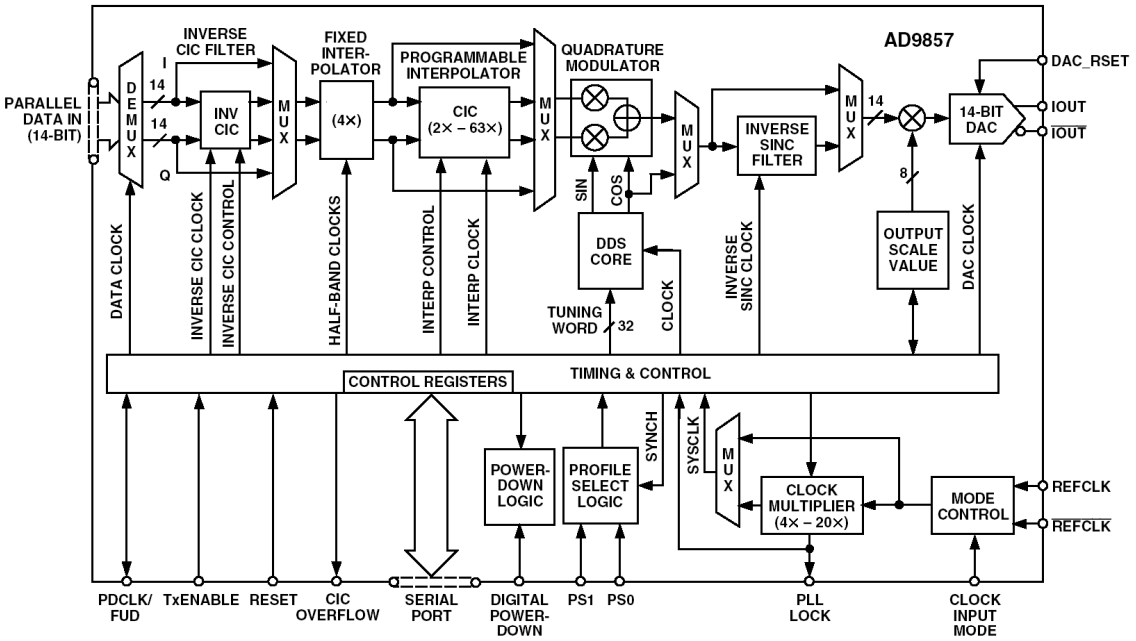


Figure 8.176: *AD9857 200-MSPS, 14-Bit Quadrature Digital Upconverter*

Parameter	AD9853	AD9856	AD9857
Master Clock	165 MHz	200 MHz	200 MHz
DAC Res	10-bit	12-bit	14-bit
Control Interface	Serial	Serial	Serial
SFDR	>50 dB @ 42 MHz (single-tone)	>80 dB Narrowband @ 70 MHz	80 dB @ 65 MHz (±100 kHz) Aout
Supply Voltage	+3.3 V to +5 V	+3 V	3.3 V
Power	750 mW @ 3.3 V	1 to 1.5 W depending on configuration	1 to 2 W depending on configuration
Package	44-MQFP	48-TQFP	80-LQFP
Notes	Complete QPSK and 16QAM Modulator	Single Tone or Modulator Mode	Single Tone or Modulator Mode

Figure 8.177: *DDS I/Q Quadrature Modulators*

REFERENCES:
8.7 DIRECT DIGITAL SYNTHESIS

1. F. M. Gardner, **Phaselock Techniques**, Second Edition, John Wiley, 1979, ISBN 0471042943.

2. Ulrich L. Rohde, Digital PLL Frequency Synthesizers, Theory and Design, Prentice-Hall, 1983, ISBN 0-13-214239-2.

3. Mike Curtin and Paul O'Brien, "Phase-Locked Loops for High-Frequency Receivers and Transmitters, Part 1, **Analog Dialogue 33-3**, 1999, http://www.analog.com.

4. Mike Curtin and Paul O'Brien, "Phase-Locked Loops for High-Frequency Receivers and Transmitters, Part 2, **Analog Dialogue 33-5**, 1999, http://www.analog.com.

5. R. E. Best, **Phase-Locked Loops: Theory, Design and Applications**, Fourth Edition, McGraw-Hill, 1999, ISBN 0071349030.

6. Richard Cushing, "A Technical Tutorial on Digital Signal Synthesis," Analog Devices, 1999, http://www.analog.com/dds.

7. David Buchanan, "Choosing DACs for Direct Digital Synthesis," **Application Note AN-237**, Analog Devices, http://www.analog.com.

8. Richard Cushing, "Amplitude Modulation of the AD9850 Direct Digital Synthesizer," Application Note AN-423, Analog Devices, http://www.analog.com.

9. Colm Slattery, "Programming the AD9832/DA9835," **Application Note AN-621**, Analog Devices, http://www.analog.com.

10. Richard Cushing, "Single-Sideband Upconversion of Quadrature DDS Signals to the 800-to-2500-MHz Band," **Analog Dialogue**, 34-3, 2000, http://www.analog.com.

11. Ken Gentile, "Digital Upconverter IC Tames Complex Modulation," **Microwaves and RF**, August, 2000.

12. Jon Baird, "400-Msamples DDSs Run on Only +1.8VDC," **Microwaves and RF**, December 2002.

13. Colm Slattery, "DDS and Converter for Signal Generator," Design Idea, **EDN**, February 20, 2003, pp. 80-82.

14. Niamh Collins, "DDS Device Produces Sawtooth Waveform," Design Idea, **EDN**, July 10, 2003, pp. 77-78.

15. David Crook, "Hybrid Synthesizer Tutorial," **Microwave Journal**, February 2003.

16. Richard J. Kerr and Lindsay A. Weaver, "Pseudorandom Dither for Frequency Synthesis Noise," **U.S. Patent 4,901,265**, filed December 14, 1987, issued February 13, 1990.

17. Henry T. Nicholas, III and Henry Samueli, "An Analysis of the Output Spectrum of Direct Digital Frequency Synthesizers in the Presence of Phase-Accumulator Truncation," **IEEE 41st Annual Frequency Control Symposium Digest of Papers**, 1987, pp. 495-502, IEEE Publication No. CH2427-3/87/0000-495.

18. Henry T. Nicholas, III and Henry Samueli, "The Optimization of Direct Digital Frequency Synthesizer Performance in the Presence of Finite Word Length Effects," **IEEE 42nd Annual Frequency Control Symposium Digest of Papers**, 1988, pp. 357-363, IEEE Publication No. CH2588- 2/88/0000-357.

SECTION 8.8: Precision Analog Microcontrollers

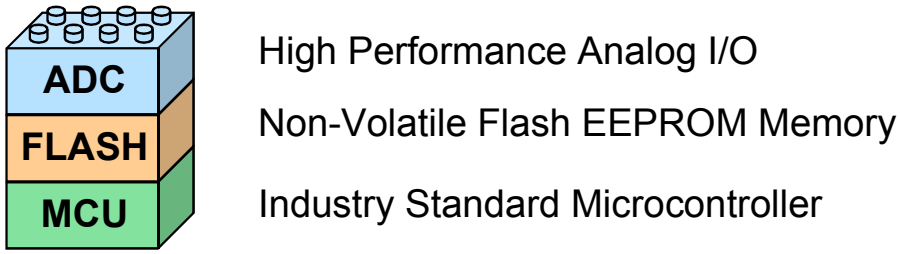
Grayson King

Introduction

Many modern sensor interfacing designs require not only precision signal conditioning and A/D conversion, but also some local embedded processing to control the ADC and perform some signal manipulation in the digital domain. Microcontrollers are ideal for this function, and the addition of non-volatile memory allows the storage of various calibration coefficients and facilitates system reprogramming. Of course, the combination of ADC, non-volatile memory, and microcontroller is useful in many other applications as well, including communications, medical, and handheld instrumentation to name just a few.

In addition, there has been considerable effort to define "smart sensors" which have standardized digital interfaces for connecting to various buses (References 1-4). Signal conditioning, A/D conversion, and microcontroller-based digital processing form the basis of these smart sensors.

Analog Devices has taken these three main ingredients and integrated them into a single chip called a "MicroConverter®." Each product in the MicroConverter family contains high performance analog I/O, non-volatile flash EEPROM memory, and an industry-standard microcontroller core as shown in Figure 8.178. In addition to these three basic functional blocks, many additional on-chip peripherals are included.



MicroConverter®

Figure 8.178: *MicroConverter® Definition*

There are many benefits to this type of integration, including smaller overall size, reduced manufacturing cost (because of reduced parts count), reduced emissions (because data buses are kept internal to the chip), and easier software design (because interface to on-chip peripherals is already done).

Characteristics of the MicroConverter Product Family

Of the approximately 15 individual 8051-based MicroConverter devices currently available from Analog Devices, about half utilize a standard switched capacitor SAR ADC architecture with 12-bit resolution and up to 400 kSPS sampling frequency. The parts are fully specified at both +3-V and +5-V supplies. Figure 8.179 shows the ADuC842 which is representative of the SAR-based MicroConverter products. In addition to the ADC, there are two 12-bit on-chip DACs and other peripherals.

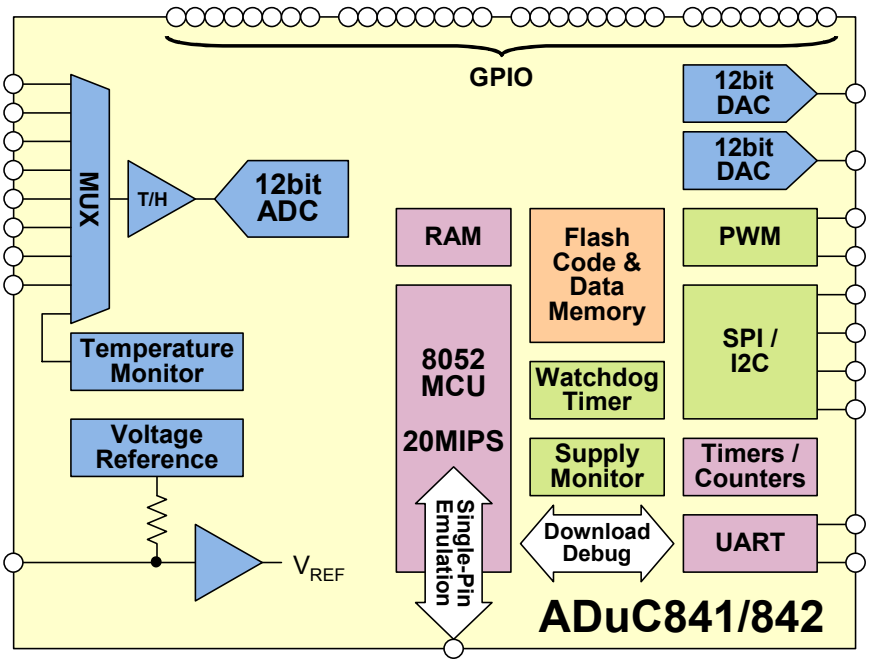


Figure 8.179: *Standard SAR MicroConverter® Products ADuC812/831/832/841/842/843*

All members of the SAR MicroConverter family have an 8-channel input multiplexer. In addition, the on-chip temperature monitor can be used to measure the die temperature. The flash memory is divided into code memory (8 Kbytes to 62 Kbytes) and data memory (640 bytes to 4 Kbytes). On-chip RAM is either 256 bytes or 256 bytes + 2 Kbytes.

The microcontroller core is the industry-standard 8051, and the processor speed is between 1 and 20 MIPS, depending on the particular device.

Figure 8.180 shows the lowest cost member of the MicroConverter family, the ADuC814 which, is housed in a 28-lead TSSOP package. When operating from 3-V supplies, the power dissipation for the part is below 10 mW.

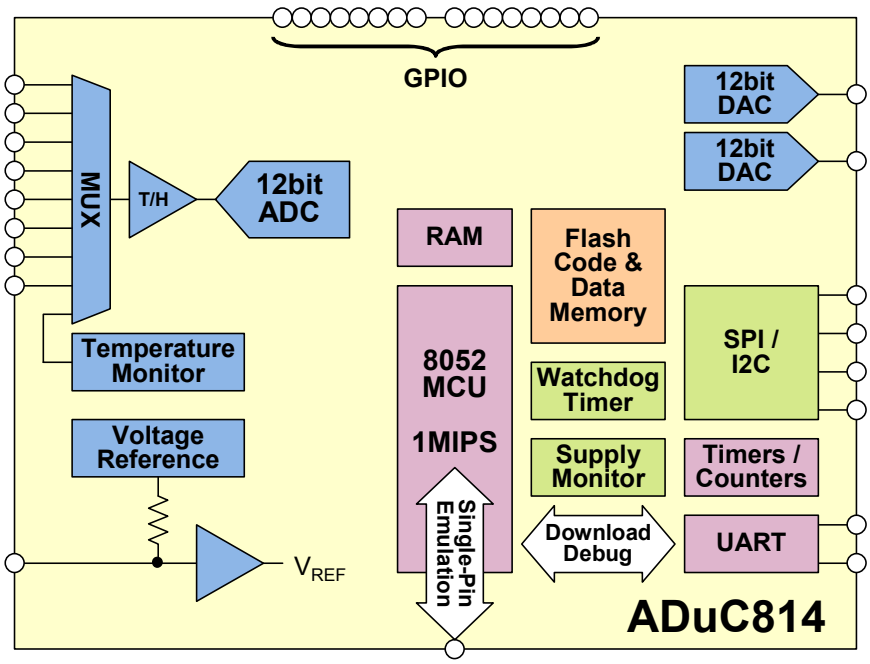


Figure 8.180: *ADuC814 Reduced Pin-Count / Low Cost SAR MicroConverter®*

The MicroConverter product family integrates precision data acquisition circuitry on the same chip as the microcontroller, without compromising performance of the analog functions. Figure 8.181 shows an FFT of the SAR ADC output with a 10-kHz input signal. Note that there is practically no degradation in ac performance whether or not the microcontroller is active. In either case, the SNR is greater than 70 dB , and the SFDR is greater than 80 dBc.

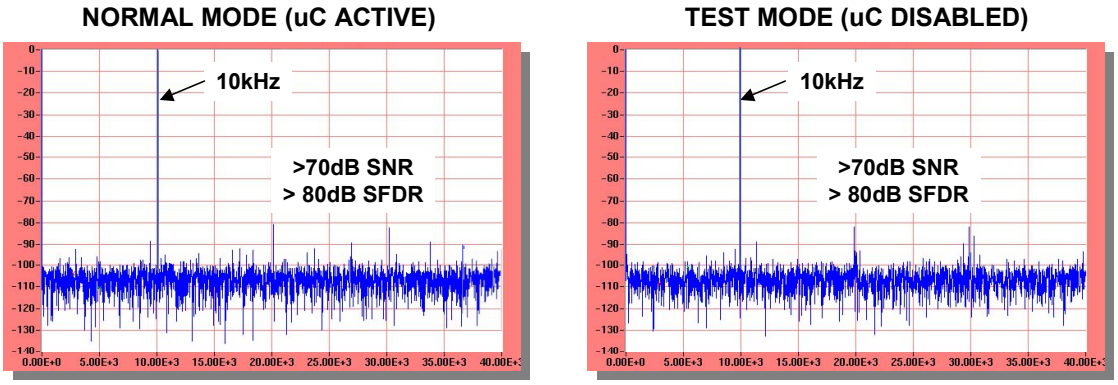


Figure 8.181: *MicroConverter SAR ADC Performance*

Figure 8.182 summarizes the 12-bit SAR-based MicroConverter family.

Part #	ADC	DAC	MCU	Flash/EE Code	Flash/EE Data	RAM	PKGs	Special Features
ADuC812	8-chan 12-bit	Dual 12-bit	1.3MIPS 8052	8K-byte	640-byte	256-byte	52-PQFP 56-CSP	Not Recommended for New Designs
ADuC814	6-chan 12-bit	Dual 12-bit	1.3MIPS 8052	8K-byte	640-byte	256-byte	28-TSSOP	Small, Low-Cost
ADuC831	8-chan 12-bit	Dual 12-bit +Dual PWM	1.3MIPS 8052	62K-byte	4K-byte	256-byte +2K-byte	52-PQFP 56-CSP	"Big-Memory" Upgrade to ADuC812
ADuC832	8-chan 12-bit	Dual 12-bit +Dual PWM	1.3MIPS 8052	62K-byte	4K-byte	256-byte +2K-byte	52-PQFP 56-CSP	Same As ADuC831, But With PLL Clock
ADuC841	8-chan 12-bit	Dual 12-bit +Dual PWM	20MIPS 8052	8K,32K,62 K-byte	4K-byte	256-byte +2K-byte	52-PQFP 56-CSP	"Fast-Core" Upgrade to ADuC831
ADuC842	8-chan 12-bit	Dual 12-bit +Dual PWM	16MIPS 8052	8K,32K,62 K-byte	4K-byte	256-byte +2K-byte	52-PQFP 56-CSP	"Fast-Core" Upgrade to ADuC832
ADuC843	8-chan 12-bit	Dual PWM	16MIPS 8052	8K,32K,62 K-byte	4K-byte	256-byte +2K-byte	52-PQFP 56-CSP	Stripped-Down ADuC842

Figure 8.182: *Summary of 12-Bit SAR-Based MicroConverter Products*

Other members of the MicroConverter family are based on a Σ-Δ ADC architecture, which is known for its low speed but very high precision. This half of the product family includes many features designed specifically for interfacing with low-level sensors. The ADuC834 block diagram shown in Figure 8.183 is well representative of these Σ-Δ based MicroConverter products. Its key analog features include a 24-bit primary ADC with buffered differential input and programmable gain, a 16-bit auxiliary ADC with unbuffered single-ended input, a flexible input multiplexing configuration, an on-chip temperature sensor accurate to about ±2ºC, an on-chip voltage reference with an option to connect an external differential reference source instead, a pair of 200-µA current sources for resistive sensor excitation, smaller excitation current sources on the primary ADC's inputs that can be used to detect open-circuit conditions at the sensor, and finally a 12-bit rail-to-rail voltage output DAC.

With the exception of the DAC, all these features are also found in our AD77xx stand-alone ADC products; but MicroConverter products like the ADuC834 also include an 8051 microcontroller, flash code and data memory, and a host of digital peripherals including serial communication ports, timer/counters, etc. Each MicroConverter product is supported by a suite of software development tools, enhanced by on-chip features that allow in-system programming and debugging, either through the chip's UART serial port, or using the single-pin emulation feature. This single-pin emulation is basically the same as JTAG from a functional point of view, but uses only one pin.

More recent additions to the Σ-Δ based MicroConverter line include devices with more analog input channels and a faster 8051 core. Specifically, the ADuC845 shown in Figure 8.184 accepts up to 10 single-ended analog inputs, or 5 fully differential inputs, or any combination thereof. Any input can be multiplexed to the primary or the auxiliary ADC, both of which are 24-bit; but only the primary ADC includes the buffered programmable-gain differential input stage.

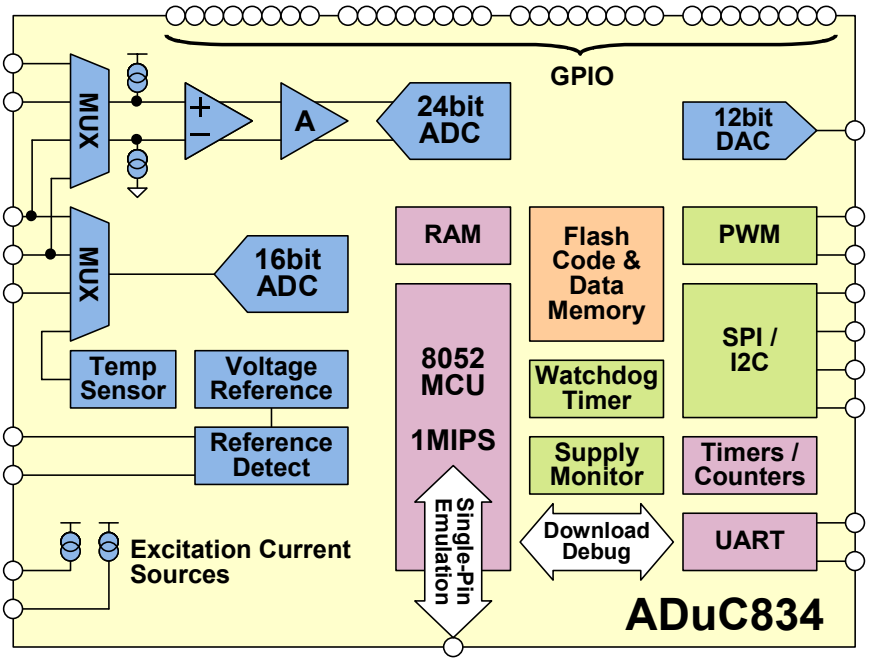


Figure 8.183: *Standard Σ-Δ MicroConverter® Products: ADuC816/ADuC824/ADuC836/ADuC834*

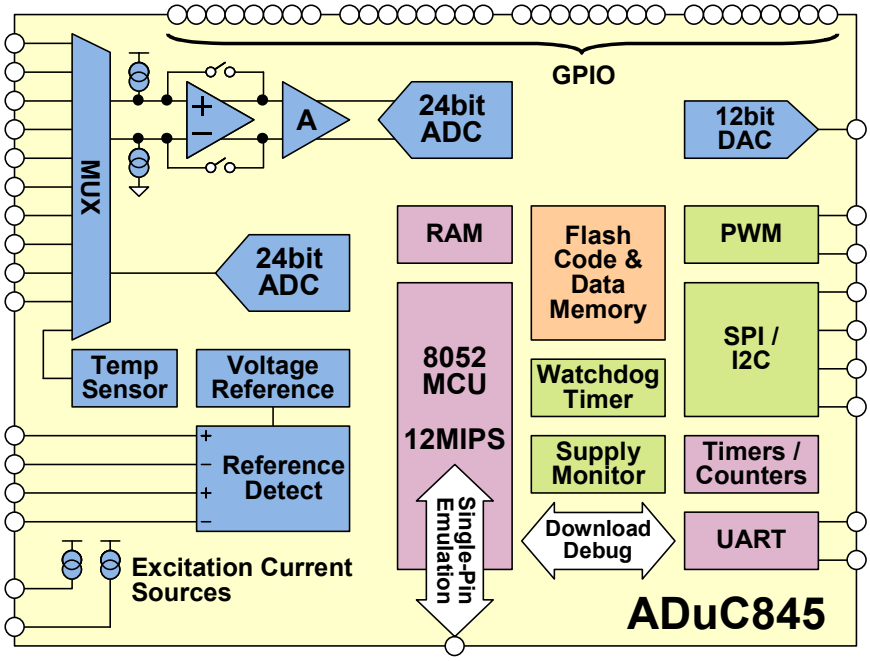


Figure 8.184: *ADuC845/ADuC847/ADuC848 High Channel-Count, Fast Core Σ-Δ Based MicroConverter*

Another unique feature of these high channel-count Σ-Δ MicroConverter products is the option to connect two completely independent differential voltage references. This is useful in multichannel applications with one or more ratiometric signal sources.

On the digital side, these high channel-count Σ-Δ MicroConverter products also feature a faster microcontroller core. Specifically, an optimized 8052 capable of over 12-MIPS peak, compared to just over 1-MIPS peak for the ADuC834. Beyond these enhancements, the ADuC845 also includes all the features of the ADuC834. However, the ADuC834 or other MicroConverter products will often provide a more cost-effective solution if the added features of the ADuC845 are not required.

As with most of ADI's high-resolution Σ-Δ converters, the conversion speed (output word rate) of Σ-Δ MicroConverter ADCs is programmable, as is their gain. Figure 8.185 shows effective resolution as a function of output word rate at the various gain settings. Output word rate can be anywhere from around 5 Hz to about 105 Hz. The noise-free code (peak-to-peak resolution) performance shown in Figure 8.185 is characteristic of all the 24-bit Σ-Δ MicroConverter products.

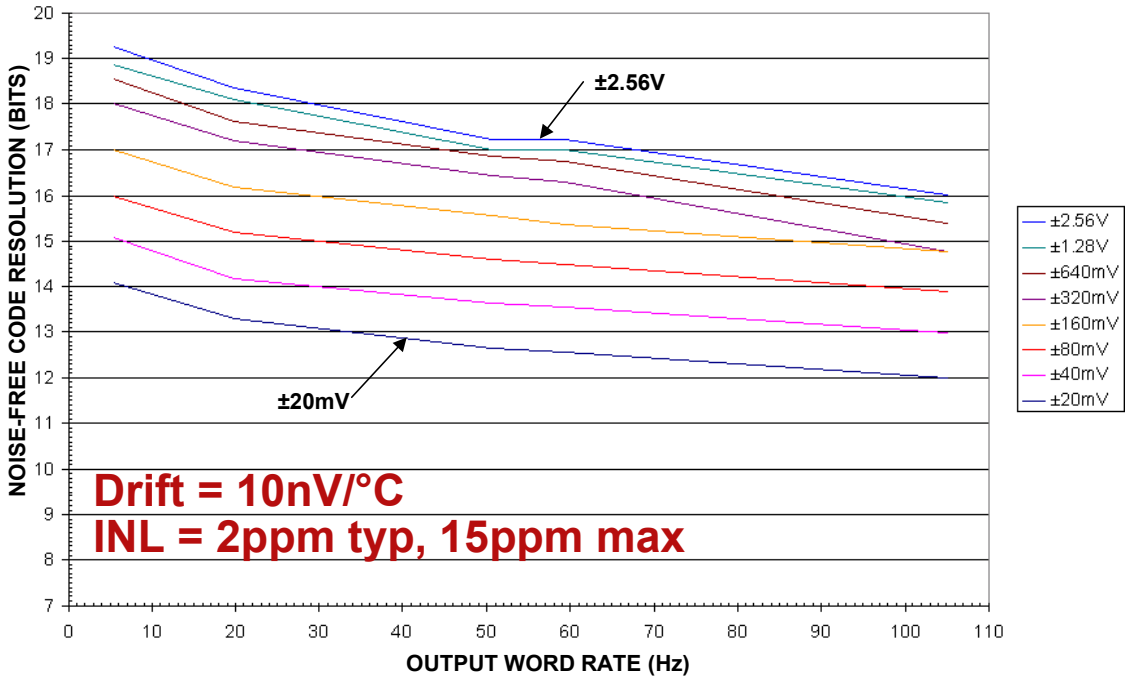


***Figure 8.185:** Σ-Δ ADC Performance – Normal Mode*

Notice that peak-to-peak resolution is better than 19 bits at the lowest gain and slowest throughput rate. This equates to an effective rms resolution of better than 21.7 bits, and makes it pretty clear that all the digital integration in these MicroConverter products has not affected their analog precision.

Furthermore, in their normal mode of operation, these ADCs employ an ADI patented chopper stabilization technique, similar to that of chopper stabilized amplifiers, to achieve unprecedented temperature drift performance. Also, built-in self-calibration features can essentially eliminate endpoint offset and gain errors.

With the high channel-count Σ-Δ delta MicroConverter products, you have the option of turning the ADC's chop-mode off. This allows much higher output word rates (up to 1.3 kHz), but at the cost of degraded effective resolution and significantly worse temperature drift performance as shown in Figure 8.186. This is a software selectable option, however, and in most applications it is desirable to leave chop mode enabled, resulting in the superior noise and drift performance shown previously in Figure 8.185.

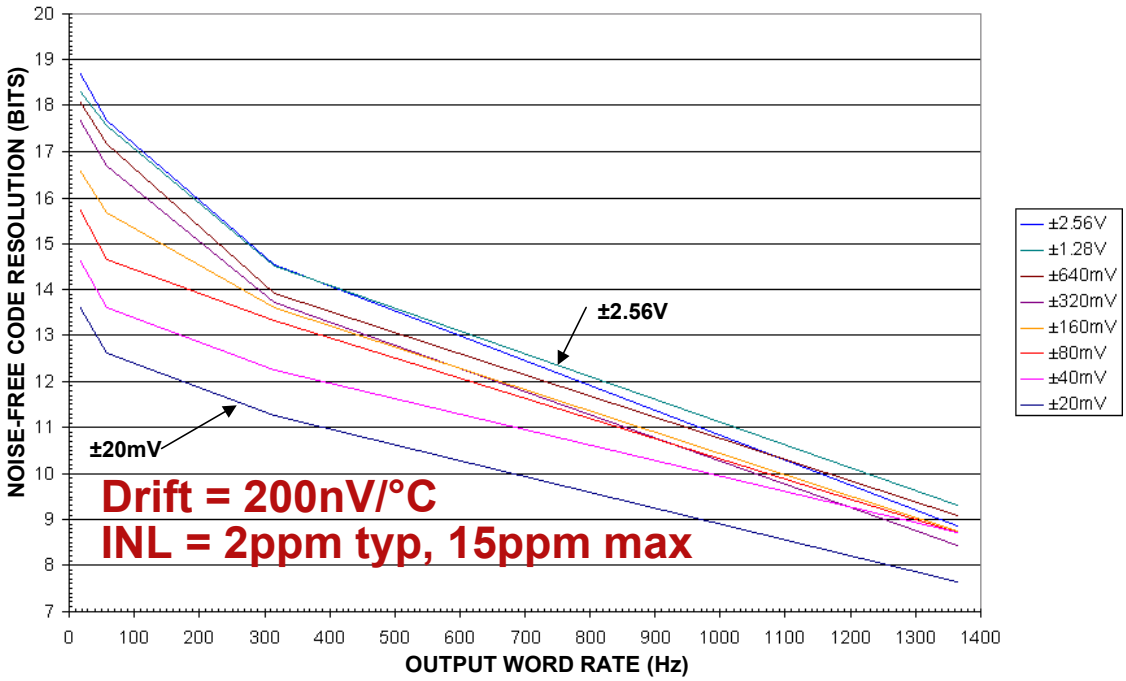


Figure 8.186: *Σ-Δ ADC Performance – Chop Mode Disabled*

The current Analog Devices' Σ-Δ MicroConverter family is summarized in Figure 8.187.

Part #	ADC	DAC	MCU	Flash/EE Code	Flash/EE Data	RAM	PKGs	Special Features
ADuC816	Dual 16-bit	Single 12-bit	1MIPS 8052	8K-byte	640-byte	256-byte	52-PQFP 56-CSP	Lowest Cost Σ-Δ MicroConverter
ADuC824	24-bit + 16-bit	Single 12-bit	1MIPS 8052	8K-byte	640-byte	256-byte	52-PQFP 56-CSP	Pin-Compatible Upgrade to ADuC816
ADuC834	24-bit + 16-bit	Single 12-bit +Dual PWM	1MIPS 8052	62K-byte	4K-byte	256-byte +2K-byte	52-PQFP 56-CSP	"Big-Memory" Upgrade to ADuC824
ADuC836	Dual 16-bit	Single 12-bit +Dual PWM	1MIPS 8052	62K-byte	4K-byte	256-byte +2K-byte	52-PQFP 56-CSP	"Big-Memory" Upgrade to ADuC816
ADuC845	10-chan 24-bit	Single 12-bit +Dual PWM	12MIPS 8052	8K,32K,62 K-byte	4K-byte	256-byte +2K-byte	52-PQFP 56-CSP	"Fast-Core" ΣΔ with Multi-Channel Input
ADuC847	10-chan 24-bit	Dual PWM	12MIPS 8052	8K,32K,62 K-byte	4K-byte	256-byte +2K-byte	52-PQFP 56-CSP	Stripped-Down ADuC845
ADuC848	10-chan 16-bit	Dual PWM	12MIPS 8052	8K,32K,62 K-byte	4K-byte	256-byte +2K-byte	52-PQFP 56-CSP	16-bit Version of ADuC847

Figure 8.187: *Summary of Σ-Δ Based MicroConverter Products*

Some Σ-Δ MicroConverter Applications

The following application examples use the ADuC834. Keep in mind that you can just as easily substitute any of the Σ-Δ MicroConverter products into any of these example configurations, depending upon system requirements.

Figure 8.188 shows a bridge transducer design using the ADuC834 that employs the ratiometric technique discussed earlier in this chapter, and therefore a voltage reference is not required. Notice that the sense lines from the bridge (connecting to the reference inputs) are wired separately from the excitation lines (going to VDD & ground). This results in a total of six wires going to the bridge. This six-wire connection scheme is a feature of most off-the-shelf bridge transducers (such as load cells) that helps to minimize errors that would otherwise result from wire resistance.

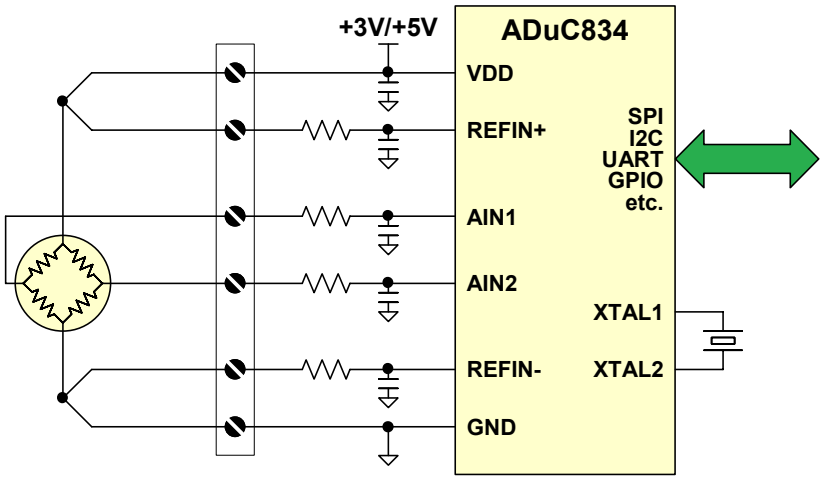


Figure 8.188: *Bridge Transducer Interfacing Using a MicroConverter*

This represents the complete design except for the serial connection to the rest of the system. No other support components are required, with the possible exception of overvoltage protection diodes at the terminal block inputs. This is an example of how MicroConverter products have earned the label, "system on a chip." The software design is facilitated by the excellent set of MicroConverter development tools.

Figure 8.189 shows a typical MicroConverter thermocouple application. Again, this is similar to the thermocouple interface to a standard Σ-Δ ADC as previously discussed in this chapter. The AD592 is used to sense the "cold junction" temperature. The calibration and linearization coefficients for the thermocouple are stored in the microcontroller memory. Since signals in this circuit are not ratiometric like they were for the bridge transducer circuit, a precision voltage reference is required. We could use the ADuC834's on-chip voltage reference, but to take full advantage of the high resolution ADC performance, it is beneficial to use a precision, low noise, external reference like the AD780.

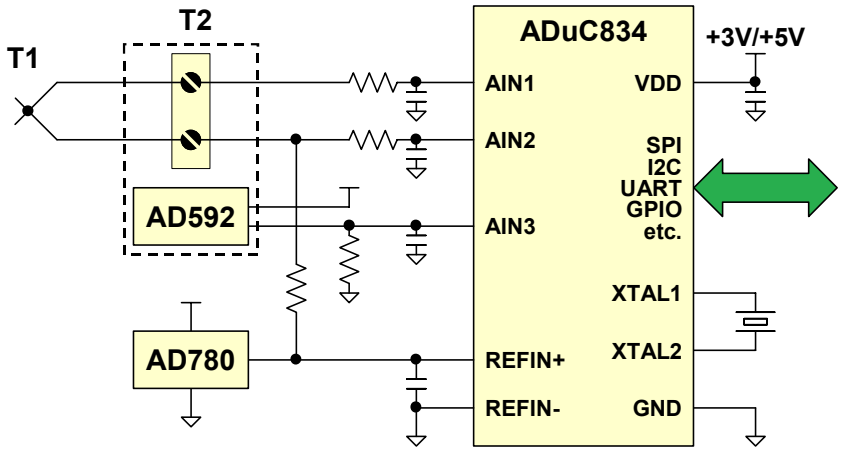


Figure 8.189: *Thermocouple Interfacing Using a MicroConverter*

Figure 8.190 shows the MicroConverter interfaced to an RTD via a 4-wire connection. Off-the-shelf RTDs are typically available in 2-wire, 3-wire, or 4-wire configurations, but the four-wire connection is the best way to minimize errors caused by lead resistance, which can otherwise be significant. Note that this is another ratiometric configuration that does not require a voltage reference. The excitation current generated in the MicroConverter (IEXC1) flows through the RTD and the R_{REF} resistor. The voltage developed across the R_{REF} resistor is used to set the reference voltage for the MicroConverter, thereby establishing ratiometric operation. The MicroConverter software is used to correct for nonlinearities in the RTD transfer function.

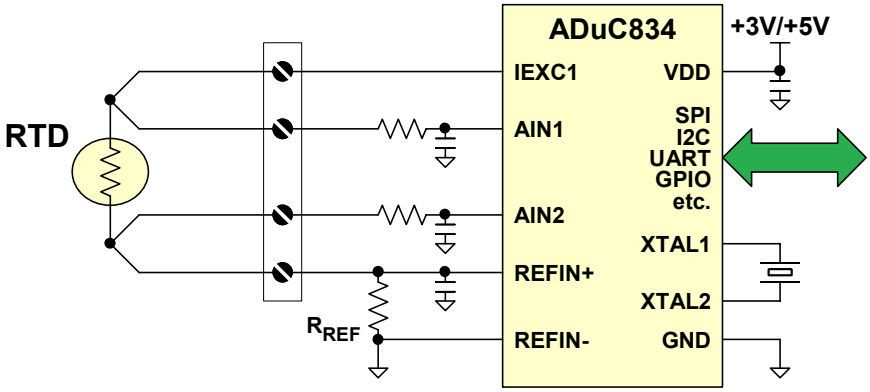


Figure 8.190: *RTD Interfacing Using a MicroConverter*

Finally, the table shown in Figure 8.191 summarizes the current 8051-based Analog Devices' MicroConverter products.

* Recommended for New Designs	12-bit up to 400kSPS		16-bit/24-bit 5.35Hz – 1.36kHz	
	SAR	SAR REDUCED PIN COUNT	Σ-Δ	Σ-Δ HIGH CHANNEL COUNT
Standard	ADuC812	ADuC814*	ADuC824* ADuC816*	
Large Memory	ADuC831* ADuC832*		ADuC834* ADuC836*	
Fast Core	ADuC841* ADuC842* ADuC843*			ADuC845* ADuC847* ADuC848*
	Pin Compatible		Pin Compatible	Pin Compatible

Figure 8.191: *ADuC8xx Product Family Overview*

A complete set of development tools for the MicroConverter product family is available from Analog Devices to facilitate software development and system integration (Figure 8.192). The QuickStart™ development kit includes an evaluation board as well as a power supply, download/debug cable, and software development tools. The QuickStart Plus™ kit features complete non-intrusive emulation capability (C-Source/Assembly).

Figure 8.192: *MicroConverter Development Tools*

ADuC7xxx MicroConverter Products Based on the ARM7® Processor Core

Although the 8051/8052 is a popular 8-bit microcontroller core, there are applications where a more powerful core is required. Analog Devices has chosen the ARM7TDMI® core for the ADuC7xxx MicroConverter product family. This popular core offers industry-standard software, and provides a 16/32-bit RISC (reduced instruction set computer) architecture. The concept for the ADuC7xxx family is similar to that of the standard ADuC8xx family, with some important added enhancements including the ARM7 core (Figure 8.193).

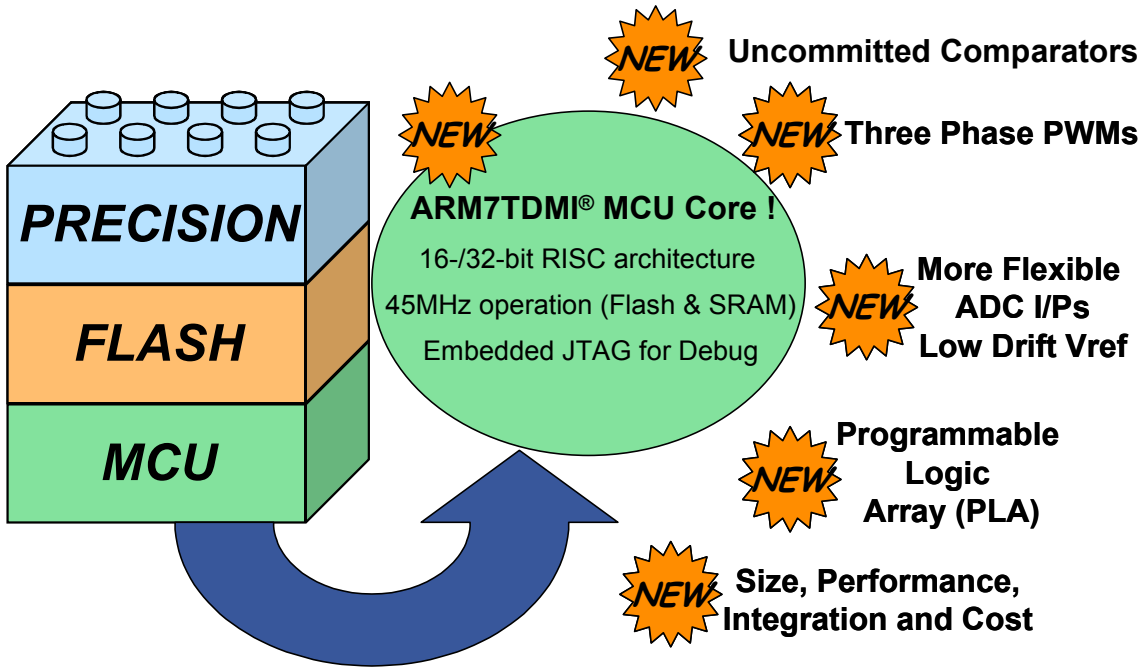


Figure 8.193: *ADuC7xxx Family of ARM7-Based MicroConverter Products*

The first group of ADuC7xxx products is the ADuC702x. A simplified diagram of the ADuC702x series is shown in Figure 8.194. The analog section has a flexible multiplexer with up to 12 standard inputs. The inputs can be configured as single-ended, pseudo-differential, or fully differential. The SAR ADC has 12-bit resolution and a sampling rate of 1 MSPS. In addition there is an uncommitted comparator, a low drift bandgap reference, and multiple 12-bit voltage output DACs. The processor core is the ARM7TDMI®, and there is 62 Kbytes of flash memory, and 8 Kbytes of SRAM. Regarding additional peripherals, there is an on-chip programmable logic array (PLA), power supply monitor (PSM), general purpose I/O (GPIO), serial I/O, general purpose timers, and three phase pulse width modulator (PWM).

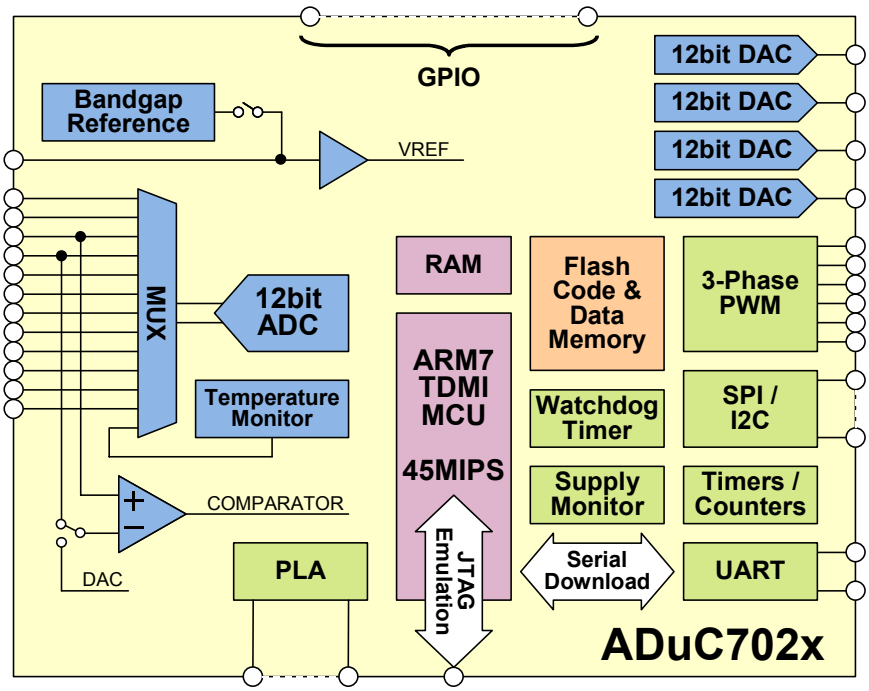


Figure 8.194: *ADuC702x ARM7-Based MicroConverter Products*

A summary of the members of the ADuC702x product family is given in Figure 8.195. The ADuC702x allows in-system programming via the UART or JTAG ports as shown in Figure 8.196, and Figure 9.197 summarizes the development system.

Part #	ADC Chnls	DAC Cnnls*	Flash (bytes)	SRAM (bytes)	GPIO (max)	Com-parator	PWM	Package
ADuC7020	5	4	62k	8k	14	Yes	No	40LFCSP
ADuC7021	8	2	62k	8k	13	Yes	No	40LFCSP
ADuC7022	10	0	62k	8k	13	Yes	No	40LFCSP
ADuC7024	10	2	62k	8k	30	Yes	Yes	64LFCSP
ADuC7026	12	4	62k (+Ext Memory)	8k	40	Yes	Yes	80LQFP

*** Unused DAC output channels can be used as additional ADC input channels.**

Figure 8.195: *ADuC702x ARM7-Based MicroConverter Product Family*

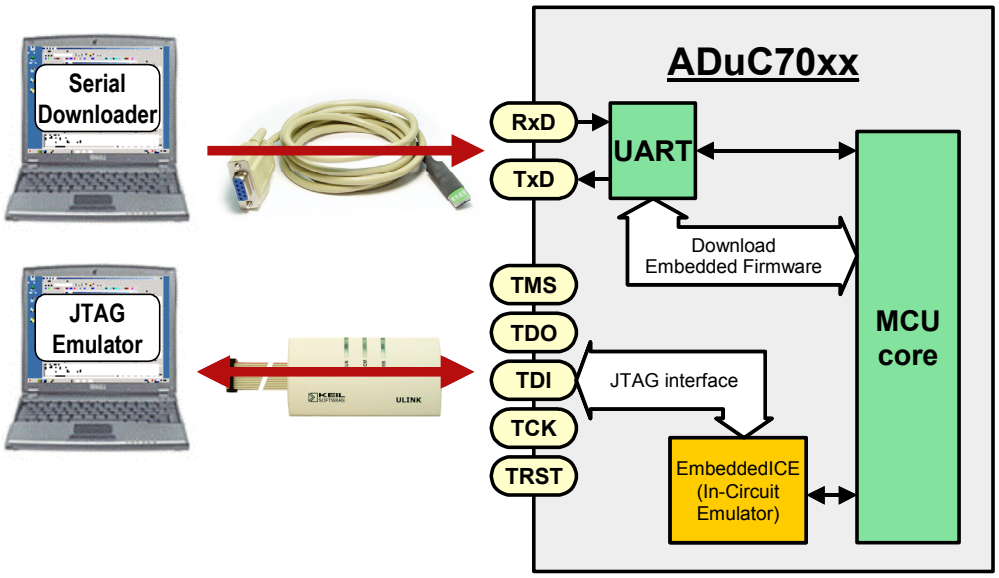
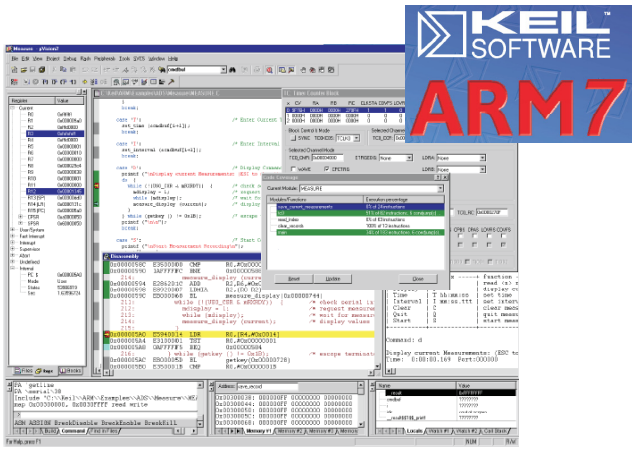


Figure 8.196: *On-Chip Tools Resources*

- Software
  - Easy to use Integrated Environment



- Hardware
  - Everything you need to get started with the ADuC70xx family

Figure 8.197: *ADuC70xx Development System*

Additional applications circuits for the MicroConverter product family can be found in References 5-13. General programming and architecture information for the 8051/8052 core can be found in References 14-18. The primary source for ARM7 information is the ARM website, http://www.arm.com (Reference 19).

The interested reader should also consult Analog Devices' MicroConverter website for additional technical notes, articles, references, sample code, etc., at http://www.analog.com/microconverter.

REFERENCES:
8.8 PRECISION ANALOG MICROCONTROLLERS

1. Alex Mendelsohn, "A Real System-On-A-Chip Needs Data Converters," **Portable Design**, June 1998.

2. Brian O'Mara and Paul Conway, "Designing an IEEE 1451.2–Compliant Transducer," **Sensors**, August 2000.

3. Brian O'Mara, "From Sensors to Networks: Microcontrollers Are Common Components In Sensor Measurement Signal Paths," **ECN**, April 2001.

4. Bill Travis, "Sensors Smarten Up," EDN, March 4, 1999.

5. Darragh Maxwell and Russell Williamson, "Wireless Temperature Monitoring in Remote Systems," **Sensors**, October 2002.

6. Mark Malaeb, "Single-Chip Digitally Controlled Data-Acquisition as Core of Reliable DWDM Communication Systems," Analog Dialogue, Volume 36, Number 5, September-October, 2002, http://www.analog.com.

7. Mark Malaeb, "Closed-Loop Control Circuit Implementation of the ADuC832 MicroConverter® IC and the AD8305 Logarithmic Converter in a Digital Variable Optical Attenuator," **Application Note AN-643**, Analog Devices, http://www.analog.com.

8. Eamon Neary, "Frequency Measurement Using Timer 2 on a MicroConverter®," **Application Note AN-644**, Analog Devices, http://www.analog.com.

9. Eamon Neary, "Interfacing an HD44780 Character LCD to a MicroConverter®," **Application Note AN-645**, Analog Devices, http://www.analog.com.

10. Luca Vassalli and Mark Malaeb, "Optical Module Development Platform 2.5 Gbps Transmitter with Digital Diagnostics," **Application Note AN-654**, Anaog Devices, http://www.analog.com.

11. Nobuhiro Matsuzoe, "Tunable Laser Reference Design for Designers with the ADuC832/ADN8830/ADN2830," **Application Note AN-655**, Analog Devices, http://www.analog.com.

12. Brian Moss, "XY-Matrix Keypad Interface to MicroConverter®," **Application Note AN-660**, Analog Devices, http://www.analog.com.

13. Brian Moss, "ADuC814 to ADM1032 via I^2C® Interface," **Application Note AN-661**, Analog Devices, http://www.analog.com.

14. Thomas W. Shultz, **C and the 8051 Vol.I: Hardware, Modular Programming & Multitasking**, Second Edition, Prentice-Hall, 1998.

15. Thomas W. Shultz**, C and the 8051 Vol. II: Building Efficient Applications**, Prentice Hall, 1999.

16. I. Scott MacKenzie, **The 8051 Microcontroller**, Third Edition, Prentice-Hall, 1999.

17. James W. Stewart and Kai Miao, **The 8051 Microcontroller: Hardware, Software, and Interfacing**, Second Edition, Prentice Hall, 1999.

18. http://www.8052.com. (*A general reference site on the 8051, 8052 microcontrollers)*.

19. http://www.arm.com. *(A general reference site for the ARM-family of microcontrollers)*.

20. Sensor Interfacing Seminar, NetSeminar, www.analog.com/mcvNetSeminar

NOTES: